

# Taming the final frontier of optical lithography: Design for sub-resolution patterning

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## ABSTRACT

The 20nm node, with a targeted wiring pitch of 64nm, is the first technology node to dip below the fundamental  $k_1=0.25$  resolution limit of high-NA 193nm immersion lithography. Double-patterning has been applied in previous technology nodes to address specific image quality issues such as line-end shortening or poor process window on contacts and vias, but never before has double-patterning been used to form images below the frequency-doubled resolution-limit of optical lithography. This paper describes the design-technology co-optimization efforts exercised by the alliance program for Bulk CMOS technology development at IBM in pursuit of cost-effective double-patterning for the 20nm technology node. The two primary double-patterning contenders, pitch-splitting and sidewall-image-transfer, are reviewed and their unique layout decomposition requirements are contrasted. Double-patterning design enablement solutions and their particular applicability to each step in the design flow are described. The paper closes with a review of the cost-effectiveness of current double-patterning solutions, highlighting the important role of design-technology co-optimization in ensuring continued cost-effective semiconductor scaling.

**Keywords:** Cost-effective double-patterning, sidewall-image-transfer, pitch-splitting, wafer-level frequency doubling.

## 1. INTRODUCTION

### 1.1 Motivation and Overview

The persistent uncertainty regarding the timely availability of next generation lithography solutions is forcing leading edge semiconductor manufacturers and their designers to grapple with the reality of having to enable sub-resolution patterning solutions. After breaking through the  $k_1=0.5$  barrier in the 65nm technology node, the rapidly approaching 20nm node will be pushing high-NA 193nm immersion lithography well below the fundamental limits even of frequency doubled optical lithography. Maintaining the industry's pace of cost-per-function scaling will rely on the development of wafer-level patterning enhancements that effectively double the lithographically achievable pattern density. While the general patterning feasibility of two such process enhancements: pitch-splitting [1] and sidewall-image-transfer [2], has been demonstrated, previous work on strong RET, such as altPSM, has also proven the need to include design ability in the overall technology feasibility assessment and optimization [3]. Resolution enhancement technology development once focused solely on process window optimization, but the times when patterning choices were completely transparent to designers are gone and the degree to which specific patterning choices impact design is becoming a decisive factor in choosing the optimal patterning process. Since frequency doubling patterning enhancements inevitably increase wafer process cost and can impact achievable chip area reduction, cost-effective technology scaling to the 20nm node and beyond will depend on detailed optimization of every step in the design-to-silicon flow.

After briefly explaining the specific double-patterning techniques being pursued for 64nm wiring pitch, this paper outlines and contrasts the topology restrictions imposed by each of these wafer-level frequency-doubling techniques. Different means of enabling double-patterning compliant designs are then proposed, highlighting the unique requirements of the different steps in the design flow. The final section of the paper discusses cost implications of

double-patterning and shows the progress that has been made in deriving a cost-effective scaling solution for the 20nm node.

### 1.2 Scaling trends and challenges

As illustrated in Fig.1, the semiconductor industry has been following a very aggressive path of scaling linear dimensions by 70% every two years. The underlying motivation for this relentless scaling, as dictated by ‘Moore’s Law’, is to double the transistor density on VLSI circuits every two years [4]. Also shown in Fig. 1 is the 5/4 offset between the two major critical dimensions that determine the density of a logic design, the device pitch and the wiring pitch. While not captured in any formal ‘law’, this device to wiring pitch ratio is quite commonly applied to many standard designs. The critical point that Fig.1 makes is communicated by the red horizontal line that shows the fundamental limit of optical lithography. With the shortest wavelength possible (i.e. 193nm), the highest NA possible (1.35), and frequency doubling resolution enhancement techniques fully applied, 80nm pitch represents a hard limit for optical lithography.

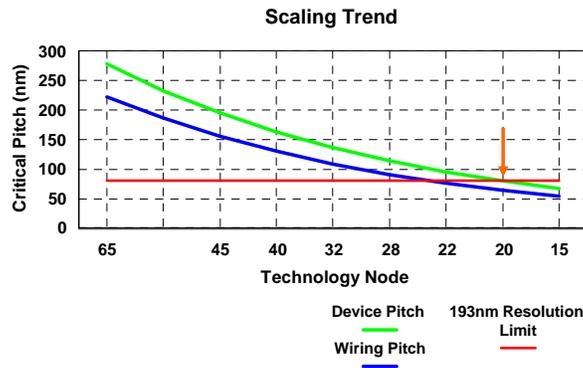


Figure 1: Semiconductor scaling trends, device pitch (green line) and wiring pitch (red line) both scale by 70% every two years to maintain the pace of transistor density increase dictated by Moore’s law. 20nm node wiring pitches lie below the fundamental resolution limit of optical lithography (red line).

The red arrow in Fig.1 shows that the 20nm node is in a very precarious position: the device pitch is at the absolute limit of optical lithography, making for extremely challenging patterning conditions, and the wiring pitch is actually below the resolution limit, putting into question the feasibility of even pursuing this technology node with optical lithography. However, the lack of timely availability of non-optical alternatives forces the investigation of sub-resolution patterning for the 20nm wiring levels. This paper focuses not on the wafer process aspects of sub-resolution patterning but on the design constraints and optimization opportunities these patterning solutions present.

## 2. SUB-RESOLUTION PATTERNING FOR THE 20NM NODE

### 2.1 Two Options for double-patterning

Cheating the resolution limit of optical lithography can be achieved by either pitch-splitting or sidewall-image-transfer as illustrated in Fig. 2. Pitch-splitting doubles the frequency of the resolvable layout by interdigitating two exposures, each having to resolve only half the ultimate pattern pitch. The concept behind this double-patterning technique is quite simple (Fig 2, left): a layout (shown in cross-section in the top of Fig. 2) is decomposed by distributing alternating features onto two photo-masks and then exposing these two masks sequentially with an optical isolation process step (such as a transfer etch or a resist freeze) to reconstruct the original image on the wafer. The most severe limitation of the pitch-splitting approach to double-patterning is the inevitable overlay error between the two exposures, i.e. since the two optically isolated images that form the final wafer pattern are exposed in independent patterning operations, mask placement, alignment, and magnification errors will cause the space between neighboring features to be adversely affected by potentially a significant amount. This coupling of critical dimension to overlay control is avoided in the sidewall-image-transfer approach to double-patterning. The frequency doubling in sidewall-image-transfer is achieved by depositing a sidewall spacer onto a mandrel shape; since every mandrel shape has two sides, the pitch of the deposited sidewalls is half that of the mandrels from which they are formed. The biggest asset and simultaneously the biggest constraint of this technique is the fact that the most critical dimension of the patterning operation is not formed lithographically, but by the deposition of the sidewall spacer. This guarantees excellent variability control, but limits the

entire layout to one critical dimension. In the specific example of sub-resolution patterning of wiring levels for the 20nm node, sidewall-image-transfer offers the options of either forming a single wire width or a single wire space. Not wanting to give up the benefits of multiple wire widths for different current loads, the foreground mode of sidewall-image-transfer, as shown in Fig.2 on the right, was chosen for this work.

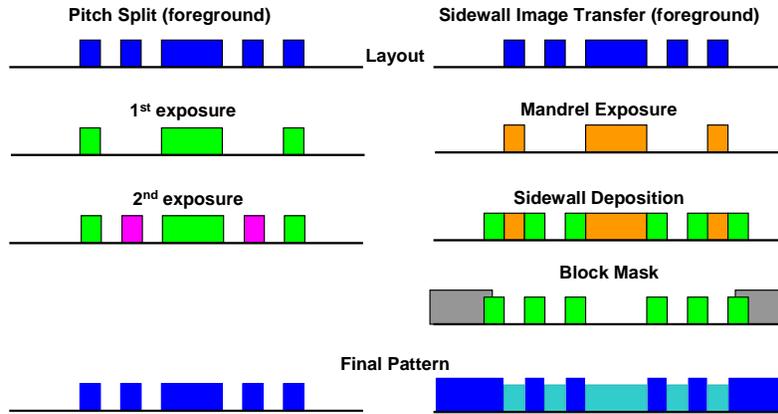


Figure 2: Two double-patterning techniques for sub-resolution lithography. Pitch splitting (left) separates the layout (top, blue) into two masks (green and purple), then recombines them with an optical isolation step in-between the two exposures. Sidewall-image-transfer (right) converts every other layout feature into a mandrel (orange) onto which a sidewall spacer (green) is deposited, doubling the pattern frequency from what had to be resolved optically. The second patterning operation of this double-patterning technique is a block mask (grey) that fills in the background in unpatterned areas of the layout.

In this particular implementation of sidewall-image-transfer, every other layout feature is turned into a mandrel using conventional lithography patterning. The deposited sidewalls then form the space, or ultimately the dielectric insulator between wiring shapes. Since even very dense layouts have more space than designed features, the second mask of this double-patterning operation serves to fill in the dielectric for all regions not formed by sidewall deposition. Fig. 2 also shows the image tone reversal that is inherent to the foreground sidewall-image-transfer process.

### 2.2 Double-Patterning Layout Decomposition

While the process integration challenges of pitch-splitting and sidewall-image-transfer are by no means trivial, some of the biggest concerns in being able to exploit wafer-level frequency doubling come from the layout decomposition step of the design flow. The two-color mapping necessary to separate layout shapes onto two masks is easily broken by common layout constructs. The simple ‘twist’ layout shown in Fig. 3a, forms an odd cycle that prevents each layout shape from being mapped onto one of two masks without features on the same mask ending up at a sub-resolution pitch. One of the outstanding advantages of pitch splitting is the fact that patterns from the two exposures can be added together to form a composite image. This ‘stitching’ capability enables coloring conflict resolution as shown in Fig. 3a.

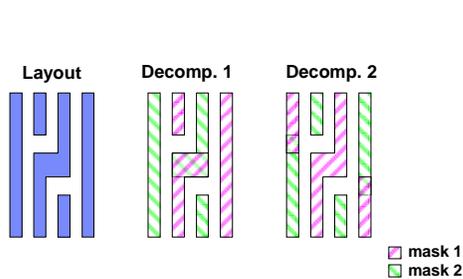


Figure 3a: Pitch splitting layout decomposition, the layout (blue) can not be mapped onto two masks without coloring conflicts, but the ‘stitching’ capability of pitch-splitting enables the two decomposition options shown.

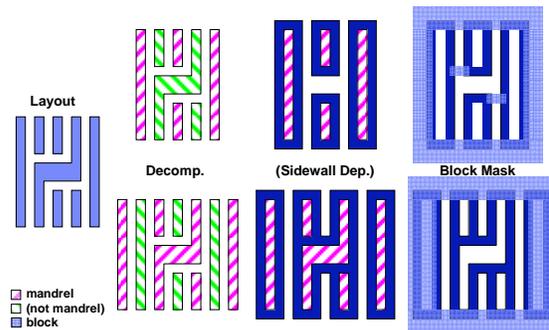


Figure 3b: Sidewall-image-transfer decomposition, features are sorted into ‘mandrel’ and ‘not mandrel’ shapes to facilitate the frequency doubling necessary for sub-resolution patterning. Dark blue outlines show the deposited sidewall and light blue shapes (far right) show the block mask.

The two-color mapping for sidewall-image-transfer is less intuitive but very similar to pitch-splitting. Rather than mapping layouts onto mask 1 vs. mask 2, for sidewall-image-transfer, the layout is mapped into ‘features formed by mandrel’ vs. ‘features formed by the absence of mandrel’. Even though there is no physical representation of ‘not mandrel’ on the wafer, it is an essential part of the two color mapping problem. A major drawback of the background implementation of sidewall-image-transfer, which allows multiple wire widths, is the fact that features can not be ‘stitched’ as in pitch-splitting. Splitting a feature into half ‘mandrel’ and half ‘not mandrel’ as was shown for pitch splitting in Fig. 3a, would result in a sidewall being deposited around the borders of the ‘mandrel’ shape; with no process steps in the flow to remove deposited sidewalls, there is no means of reestablishing electrical connectivity at the boundary between the ‘mandrel’ and ‘not mandrel’ halves of the shape. Avoiding the un-colorable odd cycle of Fig. 3a, Fig. 3b shows a two track jump which can be two-color mapped without conflict. Two coloring options are shown in Fig. 3b, illustrating the need for dummy mandrel assist features for all critical dimension lines that are not bordered by ‘mandrel’ shapes. Fig. 3 also shows the sequence of sidewall deposition and block mask patterning, leading to a reverse tone image of the original layout.

### 2.3 Double-patterning Lithography Constraints

One common misconception of double-patterning is the idea that once the layout pitch is effectively doubled through decomposition, the lithography should be very easy. Essentially, a 64nm pitch at a  $k_1$  of 0.2 is converted into two 128nm pitches at  $k_1$ s of 0.4 which should make for very comfortable printing. Unfortunately, the  $k_1$  factor alone does not adequately describe the patterning challenges of printing very small features (1/6 of the exposure wavelength) at a 4:1 duty cycle. While it is true that a lithography solution optimized for the printing of a 128nm pitch can maintain very adequate line-width-variability control over a large range of pitches, as shown in Fig. 4a, this is only true for relatively large features. Once the 64nm lines from Fig. 4a are reduced to the 32nm lines needed for double-patterning of 64nm pitch layouts, the lithography quality becomes completely unacceptable, Fig. 4b.

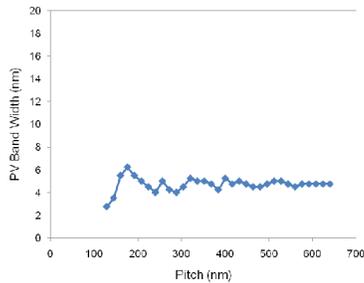


Figure 4a: Line-width variation (expressed as process-variability band width) vs pitch for 64nm openings in a dark-field mask through pitch using symmetric illumination.

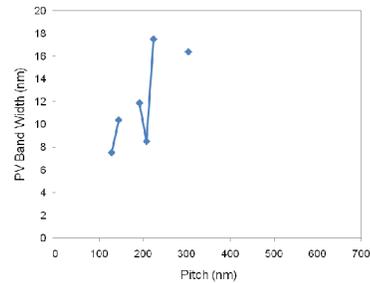


Figure 4b: Line-width variation of 32nm openings in a dark-field mask through pitch using symmetric illumination. Lack of feature biasing causes severe patterning failures.

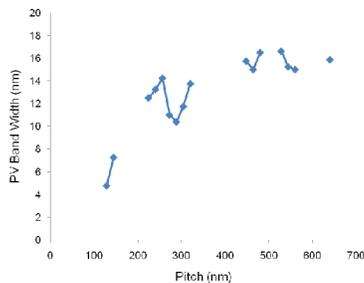


Figure 4c: Line-width variation of 32nm lines on a bright-field mask through pitch using symmetric illumination, showing patterning quality improvement over dark-field.

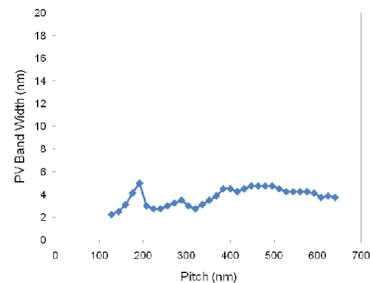


Figure 4d: Line-width variation of 32nm lines on a bright-field mask through pitch using asymmetric illumination, showing adequate image quality at the cost of preferred orientation design rules.

Reversing the tone of the image, i.e. going from 32nm wide slits in a dark-field mask to 32nm opaque lines on a bright-field mask, improves the image quality somewhat, Fig. 4c. As shown in Fig. 2, the bright-field exposure tone is actually the proper tone for a metal damascene process using sidewall-image-transfer, but the need for bright-field masks to maintain image quality requires an additional wafer-level tone inversion for the pitch-split double-patterning solution. Since the image quality shown in Fig. 4c is still inadequate, further lithography optimization comes in the form of asymmetric illumination. Switching from a quadrupole illumination to a dipole illumination substantially improves the image quality across a broad spectrum of pitches, but since a double-dipole exposure for each of the two double-patterning steps would simply not be cost-effective (requiring 4 masks for each critical metal level), asymmetric illumination drives the need for preferred orientation design rules. The important point of this discussion being that lithography-friendly design remains a requirement on top of decomposition-friendly design.

## 2.4 Double-Patterning Options for 64nm Metal

The unique attributes of pitch-splitting and sidewall-image-transfer, as they relate to design challenges, are listed in table 1. The biggest concern with pitch-splitting is the impact of overlay on critical dimension control which could easily add 5-10nm of variability to the final patterns. This concern is removed in sidewall-image-transfer at the price of a fixed critical dimension and more substantial design constraints.

	Pitch Splitting foreground	Sidewall-image-transfer foreground
DPL Masks	~ half of the features	Mandrel (every other feature)
	~ other half of the features	Block (field dielectric)
Control of Critical Dimension	overlay affects space (i.e. dielectric), introduces yield concerns	space formed by sidewall deposition, excellent control but fixed dimension
Decomposition Complexity	relatively easy	quite significant (comparable to altPSM plus assist features)
Design Constraints	limited	substantial
Conflict Resolution	easy (stitching)	limited (no stitching)
Safe Layout	preferred orientation	single orientation

Table 1: Contrasting the attributes of pitch-splitting and sidewall-image-transfer.

As detailed in the previous sections, pitch-splitting decomposition is effectively a two color mapping problem with the additional technical challenge of optimally resolving coloring conflicts by selectively inserting ‘stitch’ points. On the one hand, sidewall-image-transfer decomposition does not have to solve the stitching optimization problem (since stitching is not possible), but the requirement to design dummy assist features along with the two-color mapping, makes sidewall-image-transfer decomposition fairly challenging. A very important ‘design-ability’ distinction between these two double-patterning techniques is the lack of any means of resolving color conflicts while maintaining critical line-width control in sidewall-image-transfer, forcing more severe restrictions on this double-patterning technique. Though minor differences exist between pitch-splitting and sidewall-image-transfer, they drive a common set of design and design-flow optimization requirements that will be discussed in the following section.

## 3. DESIGN FOR DOUBLE-PATTERNING

To avoid taping-out chip designs that ultimately can not be decomposed and patterned with adequate image quality, double-patterning compliant layouts have to be enforced in the design space, similar to the way design rules and timing assertions are enforced before a design is released to the fabricator. The fact that coloring conflicts, unlike most design rule violations, are not constrained to nearest neighbor violations (i.e. odd cycle violations can occur over a large network of ‘color-related’ layout shapes with no specific point at which the color conflict originates or could be eliminated), makes enforcing double-patterning compliance more challenging than conventional design rule checking. Three primary techniques, detailed below, can be used to ensure double-patterning compatibility of a layout:

- Conventional design rules can be used in conjunction with a specialized decomposition checker. Since the complete knowledge of the double-patterning decomposition is embedded into the design operation, this approach is referred to herein as the ‘Double-patterning embedded’ design solution.
- Alternatively, designers can directly create what amounts to a manually decomposed layout by following what is referred to herein as ‘Split-level Rules’, essentially treating the two halves of a decomposed layout as separate design levels.
- Finally, prescriptive design rules can constrain the layout environment to a point where coloring conflicts are guaranteed to be impossible. This ‘Correct-by-Construction’ design solution can be implemented through restricted design rules, coarse grid layouts, or template-based designs.

As outlined in table 2, it is very conceivable that an optimal double-patterning enabled design flow draws from all three layout legalization approaches at different points in the design flow.

<b>Point in the design flow:</b>	<b>Cost-effective solution (for example):</b>
<b>Cell-level design (clean layout topologies)</b>	<b>Split-level Rules</b>
<b>Placement (cell-to-cell conflicts)</b>	<b>Correct-by-Construction (boundary conditions)</b>
<b>Routing (colored wires, colored pins/colored blockages)</b>	<b>Double-patterning embedded</b>
<b>Extraction/Timing (bimodal distribution)</b>	<b>Color-aware Timing</b>

Table 2: Different layout legalization approaches chosen for different points in the design flow to ensure a double-patterning compliant layouts.

To facilitate maximum designer creativity, custom cell level design may be best served by the ‘Split-level Rules’ while overall design flow efficiency may be best achieved through ‘Correct-by-Construction’ boundary conditions at cell placement. The inherently iterative nature of routing optimization provides a good match for a ‘DPL-embedded’ design solution. Finally, the need for color-aware extraction and timing further emphasizes the need to solve the decomposition problem in the design space. These different design legalization approaches are explained in more detail in the following sections.

### 3.1 Double-Patterning Embedded Design

The iterative double-patterning embedded design solution is illustrated in Fig. 5. A layout is checked against conventional design rules (note the preferred-orientation design allowing tighter pitch on horizontal than vertical lines), then this layout is decomposed for double-patterning and coloring violations are identified and communicated back to the designer for layout correction. In this simple example, the second decomposition check runs clean and the design is deemed legal. More complex layouts could pose very challenging layout legalization problems that require several iterations of design rule checking and decomposition checking.

### 3.2 Split-Level Rules

To avoid the complexity of iterative optimization, inherent to the ‘double-patterning embedded’ design approach, the ‘split-level’ design approach simultaneously obeys design constraints from conventional design rules and ensures decomposability by explicitly designing the layout on two design levels, Fig. 6. Two sets of design rules are provided to enable this solution: a set of intra-level rules that governs minimum dimensions and spaces of each of the two decomposition layers, and a set of inter-level rules that governs the interaction between the two decomposition levels. The difference between pitch-splitting and sidewall-image-transfer in these split-level rules is simply captured in a rule that defines the minimum required overlap between the two decomposition levels for pitch-split and forbids any overlap between these two levels for sidewall-image-transfer. A potential drawback for the ‘split-level’ design approach is the difficulty in teaching this design practice to automated layout generation or migration tools.

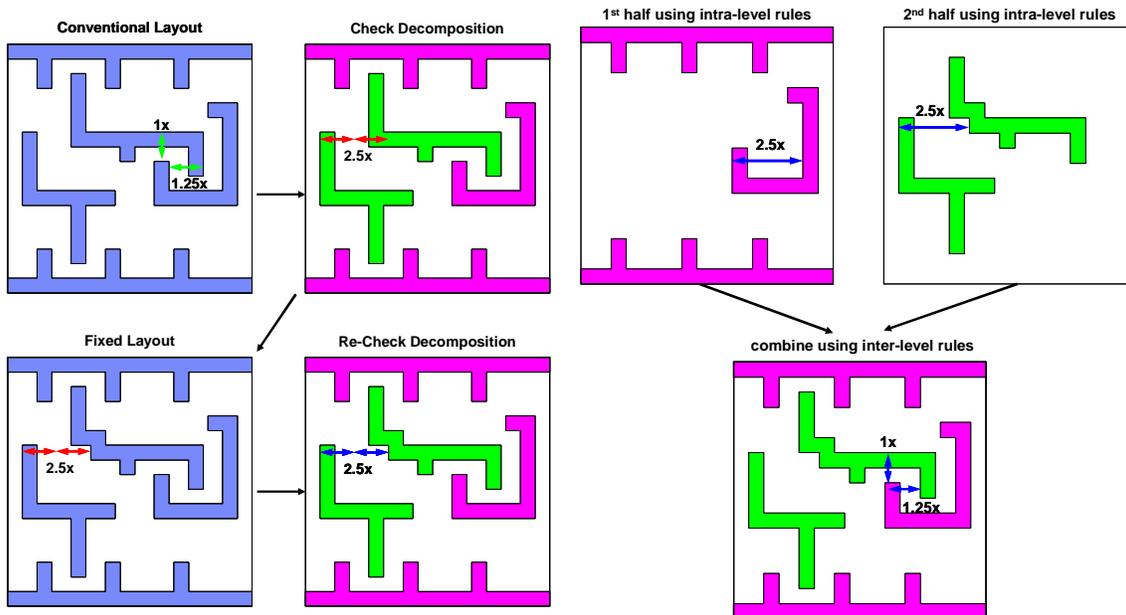


Figure 5: Double-patterning embedded design, iterative optimization of layouts by sequentially running design rule and decomposition checking.

Figure 6: Split-level design rules facilitate the simultaneous optimization to conventional design rules and decomposition constraints by explicitly designing on two levels.

### 3.3 Correct-by-Construction Boundary Conditions

Beyond the geometric topology legalization, double-patterning aware design flows also need to define methodologies to maintain design efficiency in established design automation tools. The standard-cell design methodology, widely used for ASIC designs, relies on an automatic placement tool that assembles the appropriate cells from a pre-characterized standard cell library to synthesize a physical layout from a logic netlist. It would theoretically be possible to add double-patterning awareness to this placement operation by incorporating decomposability checks as part of the placement legalization, but this would require substantial enhancements to existing placement tools and would most likely impact design efficiency and cycle time.

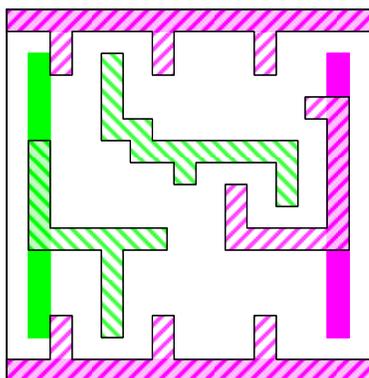


Figure 7a: Boundary conditions to ensure double-patterning aware placement. Solid shapes indicate the prescribed 'color' that layout shapes have to assume at the particular boundary.

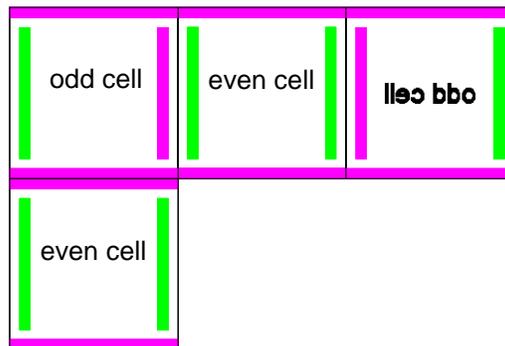


Figure 7b: Prescriptive boundary conditions help maintain design efficiency and reduce design automation tool complexity by abstracting the double-patterning awareness to a simple set of color-matching rules.

Alternatively, a set of boundary conditions, as illustrated in Fig. 7a, would maintain designer creativity inside the cell while simplifying the cell-to-cell interactions to make the double-patterning aware placement challenge more tractable. While the exact boundary conditions will depend on the specific design priorities and chosen cell architecture, Fig. 7a conceptually shows one set of boundary conditions for a 9-track cell image with shared power-rails at the horizontal cell boundaries. The top and bottom boundaries are forced to maintain the same ‘color’ to ensure that power rails can be physically connected from one cell to the next. The vertical boundaries are shown to be of uniform but opposite ‘color’, it is useful to think of this set of boundary conditions as ‘odd’ to distinguish from cells that have uniform and same ‘color’ on their vertical boundaries (i.e. ‘even’ cells). This simple set of boundary conditions allows the problem of double-patterning aware placement to be abstracted to a simple set of rules as illustrated in Fig. 7b and preserves existing circuit tuning techniques such as the ability to mirror cells for performance and density optimization.

### 3.4 Double-Patterning aware Routing

Perhaps the most complex tool in the design flow is the automated wiring tool, commonly referred to as the router. Connecting millions of pins while obeying design rules, reducing via counts, minimizing wire length, and balancing wire density across the available metal levels quickly becomes the gating factor in the extremely time sensitive ASIC design process. Introducing double-patterning compliance as an additional constraint for the router could have very serious design efficiency and cost implications. To investigate the viability of double-patterning compliant routing and to assess the most efficient means of ensuring double-patterning compatible wire topologies, the experiments summarized in Fig. 8 were conducted by the Forschungsinstitute für Diskrete Mathematik at the Rheinische Friedrich-Wilhelms-Universität Bonn, Germany. Two approaches were taken to ensure double-patterning compliant routing: a ‘color after routing’ approach in which the coloring check is done after the detailed routing solution is found, and a ‘color during routing’ approach in which the tracks in which the router runs the wires are pre-assigned alternating colors.

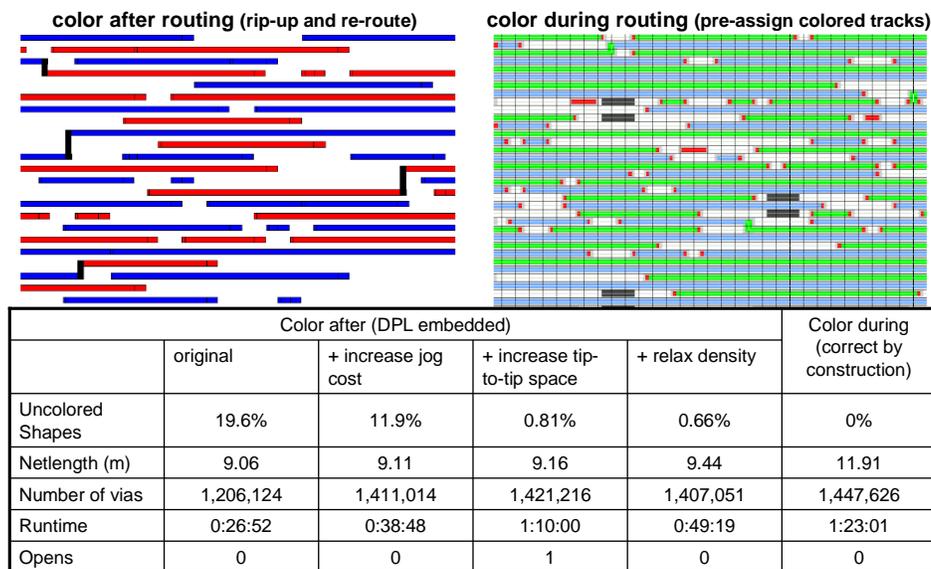


Figure 8: Comparing ‘double-patterning embedded’ (color after routing, left) and ‘correct by construction’ (color during routing, right) approaches, showing merit of either solution and providing confidence that double-patterning aware routing solutions can be developed in time for the 20nm node.

The results of this experiment showed that in the ‘color after routing’ approach, the number of color conflicts with completely un-optimized routing where substantial (19.6%) but could easily be driven to very manageable levels through existing parameters such as increasing the weight of wrong way wiring jogs in the overall routing optimization, increasing the tip-to-tip space between wiring shapes, and re-optimizing the density targets. Remaining conflicts of about 1% will be able to get resolved in an iterative rip-up and re-route optimization. One important result of this initial investigating is that a very clear set of optimization parameters: uncolored shapes vs. netlength, number of vias, and runtime can be identified to help find the optimal set of ‘color after routing’ tuning parameters. The ‘color during routing’ experiments on the same design showed that correct by construction, while yielding a fully double-patterning compliant wiring solution with no iteration, does not produce the same routing quality as the iterative ‘color-after

routing' double-patterning embedded solution. More work is needed in this area, including demonstrations of the actual rip-up and re-route iterations, addition of redundant via constraints, and the coupling of double-patterning aware routing to double-patterning compliant cells through colored pins and colored wiring blockages. But these initial results provide assurance that a double-patterning compliant routing solution can be developed in the timeframe necessary to intercept the 20nm node.

### 3.5 Double-Patterning aware Timing

The challenges of design for double-patterning are not limited to physical topology legalization. Composing a layout from two separate exposures introduces systematic variability that has to be investigated to assess its potential impact on circuit limited yield [5]. Pitch-splitting combines two exposures, each with its own random line-width variation distribution and a finite offset in nominal dimension as well as an overlay shift between the two. Sidewall-image-transfer eliminates the overlay component but still forms one set of wires by 'mandrel' the other set by 'not mandrel'. Therefore one set of wires suffers only the line-width variation of the mandrel while the other set suffers the combined variation of the mandrel and the sidewall deposition. Since the thickness of the sidewall deposition is controlled to atomic levels, it is expected that bimodal line-width distribution will not be a factor in sidewall-image-transfer, making the timing impact potentially the most decisive distinction between the two double-patterning techniques. Fig. 9 shows some early results of pitch-splitting aware timing investigations done at IBM's Austin Research Laboratory. The plots compare the simulated RC variability of the last wire in a 5 wire cluster patterned with pitch-splitting at a 10% line-width and wire-thickness variation as well as 5nm overlay error. The significant increase in RC variation for pitch-splitting is very obvious. To fully understand the impact of this additional spread in RC variation on circuit limited yield and chip performance, work is continuing with a focus on selecting specific design test-cases for rigorous analysis, investigating correlations amongst wires (e.g. clock vs. data path), and adjusting variability assumptions to quantify the timing impact difference between pitch-splitting and sidewall-image-transfer.

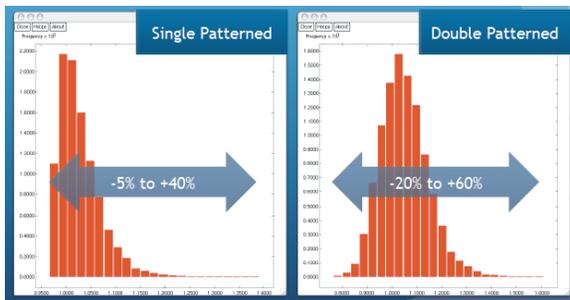


Figure 9: RC (resistance x capacitance) variation of the last line in a 5 line bundle assuming 10% line-width and wire height variation ( $\sigma$ ) and 5nm overlay error using a 2D field solver to calculate the capacitance and a simple analytical equation to calculate the resistance. Significant timing impact of pitch-splitting double-patterning may be inevitable.

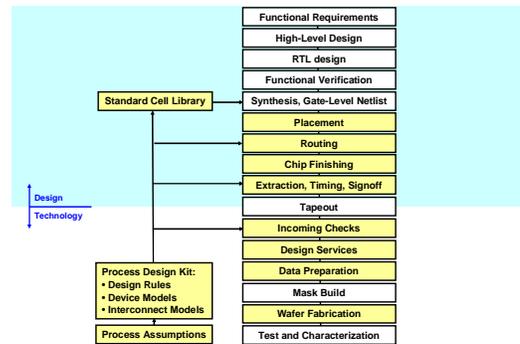


Figure 10: The impact of double-patterning can be seen in almost every aspect of the design flow (highlighted boxes).

### 3.6 Pervasive Impact of Double-Patterning

As the sections above illustrated, double-patterning affects nearly every aspect of the design flow, Fig. 10. Process design kits provided by the fabricator to the designer need to include double-patterning compliance rules and decks, the IP providers need to generate a standard cell library that is optimized for double-patterning, synthesis-place-and-route are all affected by additional coloring constraints, extraction and timing need to consider additional systematic variability sources, and –not discussed herein- the entire mask data preparation and computational lithography flow will be significantly affected by double-patterning. This pervasive impact of double-patterning provides significant technical challenges and adds to the development time-line of a double-patterning enabled technology node, but it also provides a means of deep design-technology co-optimization that is central to achieving the cost-effectiveness required to make double-patterning a viable scaling solution.

## 4. COST-EFFECTIVE DOUBLE-PATTERNING

A major motivator for the relentless density scaling that drives the semiconductor industry towards complex solutions like double-patterning is the economics of being able to double the number of transistors that can be produced at a given wafer cost. As Moore's law dictates, node-to-node transistor density should double while the cost to manufacture a wafer's worth of chips remains unchanged. This exponential improvement in cost-per-function is being challenged by the need for double-patterning due to increased mask and processing cost.

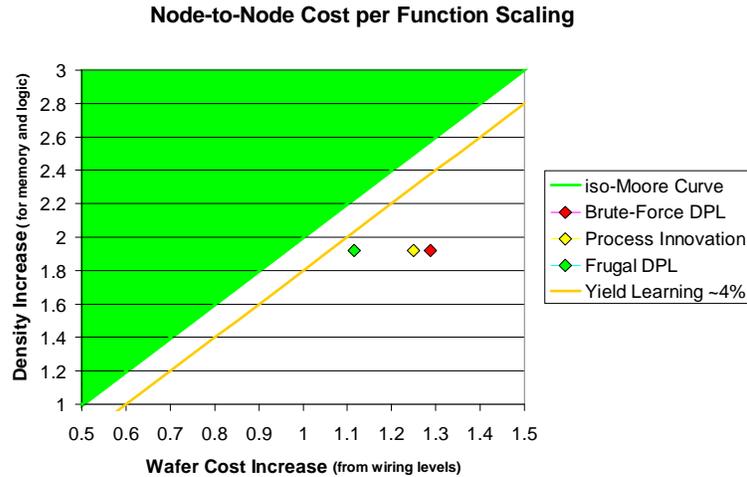


Figure 11: The cost-efficiency plane, anything above and to the left of 'twice the density at fixed wafer cost' maintains cost-effective scaling. Process and design optimization reduces the wafer cost increase for double patterned wiring from 30% to just over 10%, putting it in range of established cost scaling targets.

The ideal scaling target of twice the density at fixed wafer cost is shown in the center of Fig. 11. Realistically, any solution on the green side of the density vs. wafer cost curve would be considered 'cost-effective', i.e. higher wafer cost in return for higher density could be tolerated and, to a degree, less density improvement at reduced wafer cost could also be acceptable. As feared, the initial density and cost assessment of a double-patterning wiring solution for the 20nm node placed this solution deep into the lower right half of the density vs. cost curve, red data-point in Fig 11. Doubling the exposures for 8 metal levels and their associated via levels causes an almost 30% wafer cost increase from the wiring levels alone. Additionally, design constraints imposed by double-patterning reduce the achievable density gain by almost 10%. Reducing the cost of the double-patterning wafer processing by removing intermediate etch operations and using resist images in approaches such as litho-freeze-litho-etch [6-9] for pitch-splitting or resist-based mandrels for sidewall-image-transfer, reduces the wiring level cost increase to 25%, yellow data-point in Fig. 11. Further cost optimization involves careful selection of specific wiring levels that most benefit from the tighter wiring pitch provided by double patterning. In close collaboration with the design teams, the overall chip density can be maintained with significant reduction in the number of mask levels being double-patterned, resulting in a wafer cost increase of just over 10%, green data-point in Fig. 11. Considering that traditionally a 10% wafer cost increase node-to-node has been acceptable in light of yield improvements due to critical area reduction, the gap between current cost estimates and cost-efficiency targets closes even further, orange line in Fig. 11. The current cost analysis indicates that, for the design investigated here, a density improvement of only 3.25% over current estimates would be necessary to completely achieve the cost-efficiency goals. It has been shown that density improvement of 5-10% is very much achievable through careful design-technology co-optimization [10]. While this work can not claim to be comprehensive and final, this early analysis gives hope that cost-effective double-patterning can be achieved. However this work also shows that double-patterning can not afford to be implemented with any detriment to density or yield otherwise cost-efficiency quickly erodes. Double-patterning aware design flows have to accommodate yield enhancing features such as redundant vias and can not afford to give up density to overly conservative design restrictions.

## 5. CONCLUSION

The work presented here shows that, while posing significant challenges across the entire design flow, sub-resolution patterning using either pitch-splitting or sidewall-image-transfer is technically and economically viable. The choice of specifically which double-patterning technique to use will depend on the results of further process development and more detailed timing impact investigation. It is possible that the ultimate double-patterning solution will leverage the less restrictive layout decomposition of pitch-splitting for more two-dimensional local wiring levels while taking advantage of reduced timing impact of sidewall-image-transfer for the longer wires of inter-cell and inter-macro wiring levels. Regardless of the specific patterning option, a robust and cost-effective double-patterning solution will require complete integration of design rule generation, IP optimization, standard cell placement, routing, timing, and mask data-preparation. The reward for solving this complex integration challenge is a patterning solution that does not expose semiconductor scaling to the schedule risk associated with next generation lithography.

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