International Conference on Space Optics—ICSO 2014

La Caleta, Tenerife, Canary Islands

7-10 October 2014

Edited by Zoran Sodnik, Bruno Cugny, and Nikos Karafolas



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International Conference on Space Optics — ICSO 2014, edited by Zoran Sodnik, Nikos Karafolas, Bruno Cugny, Proc. of SPIE Vol. 10563, 1056337 · © 2014 ESA and CNES CCC code: 0277-786X/17/\$18 · doi: 10.1117/12.2304235

HIGH-THROUGHPUT OPTICAL INTER-BOARD INTERCONNECTS FOR NEXT-GENERATION ON-BOARD DIGITAL TRANSPARENT PROCESSORS

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I. INTRODUCTION

The satellite telecommunication sector is continuously facing new challenges. Operators turn towards increasing capacity payloads with higher number of beams and broader bandwidth, in order to cope with exhausting orbital positions and to lower the cost of in-orbit delivery of bit. Only satellites able to provide high data rate connections to numerous users are expected to achieve affordable communication prices. On the other hand, as the telecom market grows and the range of offered services (HDTV, Video On Demand, Triple Play), operators call for more versatile solutions to quickly grasp new markets and to adapt to these evolutions over the average 15 years of a satellite lifetime.

Flexible payloads have found an increasing interest for a number of years. Flexibility is considered as a means for a better commercial exploitation of a satellite fleet and a better allocation of resource in response to traffic evolution and/or changing business plans, with potential advantages such as a wider range of applications, less customization for specific missions, increased production runs of equipment, enhancement of reliability, reduction of equipment cost, reduction of program schedules [1]. Flexibility is expected to be offered in spectrum management and frequency plan, in coverage, or in the repeater power allocation.

The industry is taking up the challenge both by improving current telecom satellites and offering new payload technology, more flexible and able to address the new markets. From a system integrator perspective, flexibility is as an opportunity to design more generic payloads, that can be customized during or after fabrication only, thus shortening the design-to-manufacturing cycle, and improving the industry competitiveness.

II. NEXT-GENERATION ON-BOARD DIGITAL PROCESSORS

New payload designs are thus needed to meet these new requirements of larger bandwidth, transparency and flexibility. Conventional GEO-based satellites were based on a single (or a few) antenna coverage and transparent RF payloads in C and Ku bands with fixed uplink-to-downlink interconnection. Larger bandwidth is being made available through the implementation of multiple spot-beam coverage with frequency reuse and migration to Ka-band.

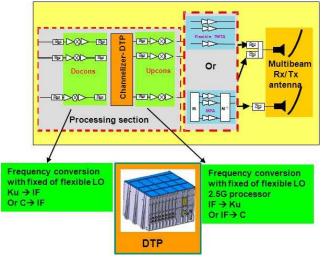


Fig. 1 : Block diagram of a transparent flexible multi-beam payload after [2]

TAS presented different concepts [2] offering a wide range of payloads solutions, together with the building blocks developed within the FLIP (FLexible Innovative Payload) project. A typical flexible multi-beam payload will achieve beam to beam connectivity thanks to a digital channelizer also known as Digital Transparent Processor (DTP) which supports channelization of input frequency bands and routing of each channel between beams. Frequency converters perform direct frequency down and up conversion between RF accesses and the DTP with input and output accesses at IF frequencies. The output section is based either on conventional TWTAs or flexible TWTAs (enabling to tune saturated output power) or on a MPA (multiport amplifier = bank of power permitting to exchange power within a set of beams).

The DTP is the most typical example of advanced telecom on-board processors. DTP's feature analogue-todigital (ADC) and digital-to-analogue converters (DAC) at their input and output accesses, and make extensive use of digital processing to provide flexible transparent connectivity and programmable bandwidth allocation.

In the frame of the ARTES 3 program, TAS qualified a DTP of 2^{nd} generation (2.0 G DTP) with a particularly high level of modularity [3]. This was achieved through an overall architecture based on the assembly of dedicated units, namely receiver chains including the A/D conversion, transmitter chains including the D/A conversion, digital filtering, gain control and routing units, DC/DC converter boards, clock generation boards, and a dedicated interface board. Thus, each DTP configuration can be easily adapted to specific needs (platform, frequency, number of inputs or outputs ...), which enables to tailor the mass and volume budgets to each mission. As a matter of example, the DTP can connect up to 20 inputs to up to 20 outputs, but the number of inputs is scalable from 2 to 20, independently of the number of outputs that can also range from 2 to 20. Other examples are shown in Fig. 2 hereafter.

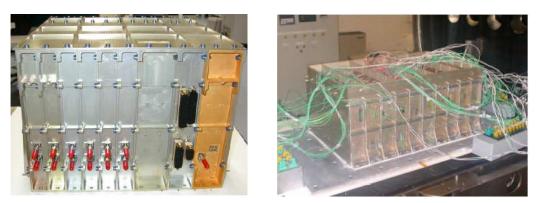


Fig. 2 : TAS Digital Transparent Processors of 2nd generation (DTP 2G)

High-speed digital processors are expected to be widely spread in future telecom repeaters and thus a technology breakthrough is required to support the expected huge amounts of data. The aggregate throughput required to interconnects in such future DTP's is a function of the bandwidth per access port and the number of accesses. To give a rough order of magnitude, when these parameters are concurrently increased, the required aggregate throughput rapidly reaches and exceeds the 1 Tbps range. Most ambitious projections look at payloads featuring more than 100 beams with up to 1 GHz bandwidth per beam. If a fully digital processing approach is adopted, this may result in a total throughput of several Tbps.

Serial electrical links may partially solve some of the above issues, by enabling to increase the bandwidth while reducing the number of connections between PCB's. They will support gigabit-per-second data rates and offer higher connection densities. As transmission speeds reach a rate where electrical data transmission between racks or stack assemblies is then becoming critical, extension technologies involving equalizing circuits may be necessary in order to maintain signal integrity. Nevertheless, the price to pay in terms of mass is quite high. Whereas this may not be a concern for terrestrial applications, the mass is very critical for space applications and any interconnect solution resulting in substantial mass savings will be paid thorough attention.

III. HIGH-THROUGHPUT OPTICAL INTERCONNECT DEMONSTRATOR

TAS has investigated optical interconnects as an enabling data communication technology for supporting the huge data throughputs expected to take place in future on-board digital processors and especially in the highly demanding DTP, not only as an equipment back-plane but also as an inter-equipment communication means. In

the past, TAS developed early optical interconnect breadboards [4] featuring tens of optical links each operating at up to 2.5 Gbps to assess the technology available at that time.

Under the ESTEC contract N° 22018/08/NL/NA *Optical Inter-board Interconnects for High Throughput on-Board Processors (OI2)*, Thales Alenia Space has been cooperating with VTT, D-Lightsys, Patria and DAS Photonics, with the objective to design, develop and test a breadboard demonstrator of a very high-density high-capacity optical interconnect solution suitable for application in advanced digital transparent processors. Taking into account the needs of the next generations, it was considered necessary to assess the capability and reliability of advanced optical interconnect technology and solutions, where the passive optical interconnection shall be able to host over 1000 links and where the total data throughput between PCBs via the interconnect plane shall be in the range of 350 Gbps in and 350 Gbps out.

Key optoelectronic modules were developed including multi-channel transceivers, transmitters and receivers. An optical interconnect demonstrator was designed and assembled to prove all the components developed within the project in a system environment. The mechanical structure of the DTP of 2nd generation (2.0 G DTP) was selected as the bed for the optical interconnect demonstrator due to its high level of modularity. The optical interconnect demonstrator architecture was based on 10 slices mimicking the dedicated units of the DTP and an optical interconnection plane. In order to minimise the development effort, three slices only were developed but all different from each other.

The first, so-called Rx/Tx slice featured:

- A Rx/Tx board integrated in the slice with
 - Multi-channel optoelectronic transmitters (Tx) and receivers (Rx) from D-Lightsys upgraded from already designed modules for space application. These modules have been designed to support 12x10 Gbps.
 - Multi-channel optoelectronic transceivers from VTT upgraded from already designed modules for space application. These modules support 4x10 Gbps for the transmitter side and 4x10 Gbps for the receiver side.
 - Thermal resistors to simulate ASIC dissipation (up to 80W in total) as well as their thermal management system of a fully populated processor board.
 - Electrical interposer to interconnect the optoelectronic modules to the PCB board
- High-density, multi-fibre optical connectors mounted on the slice, and support connections to the interconnect plane. These connectors are based on MT-ferule. Standard MT ferules support 12 fibres each. We demonstrate 16 MT ferules per board can be accommodated, thus providing up to 192 optical fibre channels per slice.
- Optical test in/out interface, in order to measure the optical insertion losses, for the optical connectors, the optical interconnect solution, the couplers, and generally speaking, the overall optical link losses.
- Electrical test interfaces to test end-to-end links representative of functional links between two ASIC's with integrated HSSL for example. Electrical test interfaces are implemented on the front panel thanks to high speed connectors. BER tests can thus be done by feeding transmitters with PRBS signals.

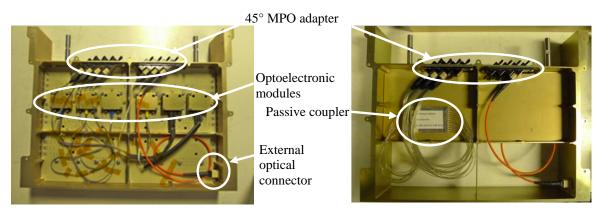


Fig. 3 : Views of the Rx/Tx slice (left) and of the passive coupler slice (right)

The second slice hosted the passive optical couplers, and was based on the same mechanical structure as the Rx/Tx slice on which the passive module is screwed and its optical fibres are connected to a dedicated 45° optical connector. No electrical signal passed through the board. Fig. 3 above show photographs of the developed Rx/Tx and passive coupler slices, respectively on the left and right side.

The last slice was a dummy slice, with similar mechanical structure as Rx/Tx slices but without any PCB board and components and with ballast in order to mimic a functional slice.

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An optical interconnect plane was developed to route the fibre links generated and terminated in Rx/Tx slices, based on flexible optical circuits (flexes) glued on a plate and equipped with multi-fibre connectors (Fig. 4).



Fig. 4 : View of the optical interconnect plane

IV. DEVELOPMENT OF KEY OPTOELECTRONIC AND OPTICAL COMPONENTS

New developments were carried out by VTT and D-Lightsys in order to upgrade optoelectronic devices they already designed for harsh environments [5] [6] into space-qualifiable modules operating at high bit rates. This included 12-channel transmitter and receiver modules by D-Lightsys, and 4-channel transceiver modules by VTT. Both VTT and D-Lightsys developed modules supporting up to 10 Gbps per channel over multimode fibre ribbon pigtail incorporating state of the art 850 nm GaAs VCSEL arrays and/or GaAS PIN photodiode array. All transmitter, receiver and transceiver multi-channel modules came in very similar small-size, hermetic ceramic package with a specific feed-through for multi-fibre ribbon pigtail, that are shown in Fig. 5. All were also designed for low power consumption which was specified at less than 10mW/Gbps per channel (including Tx and Rx).

In parallel, DAS-Photonics developed a passive optical coupler array module. It consisted in a ruggedized, small and lightweight package to house 12 individual passive 1x2 optical splitters, that was equipped with MPO male multi-fiber optical connectors as shown in Fig. 6 above.

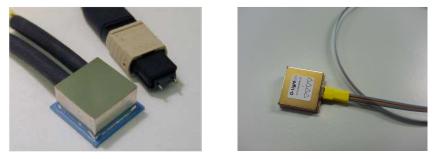


Fig. 5 : Multi-channel optoelectronic modules by VTT (left) and-Lightsys (right)

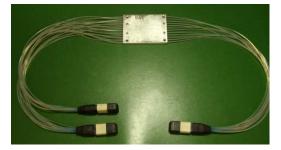


Fig. 6 : Passive optical 12-splitter array module

The adoption of optical interconnect technologies in future on-board processing units calls for hi-reliability components able of withstanding space conditions. This is the reason why the optoelectronic and passive modules were assessed according to a complete program including functional testing, thermal testing at cold and

hot temperatures, life testing and radiation testing according to the sequence and conditions detailed in Table 1 hereafter.

Table 1 : Testing sequence and conditions for optoelectronic and passive modules

Optoelectronic modules

Sample group 1		Sample group 2		Sample group 3	
Funct. test at room T°	+23°C	Funct. test at room T°	+23°C	Radiation test	
Funct. test hot T°	+70°C	Life testing	1000h/125°C	Funct. test at room T°	23°C
Funct. test at cold T°	-10°C	Funct. test at room T°	+23°C	TID	< 100krad
Funct. test at room T°	+23°C			Funct. test at room T°	23°C
		-		Proton displacement	$< 10^{12} \text{ p/cm}^2$
				Funct.l test at room T°	23°C

Passive coupler modules

Sample 1		Sample 2		
Insertion loss at room T°	+23°C	Radiation test		
Insertion loss at hot T°	+70°C	Insertion loss at room T°	23°C	
Insertion loss at cold T°	-10°C	TID	< 100krad	
Insertion loss at room T°	+23°C	Insertion loss at room T°	23°C	

As a matter of example, Fig. 7 hereafter gives the distribution of the optical output power in a 12-channel transmitter module. Measurements were done using the same bias and modulation settings for all the channels. Significant optical power level variations were observed over the different channels, evidencing that bias and modulation current conditions have to be tuned for all lasers.

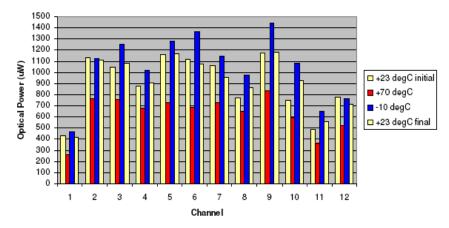


Fig. 7 : Optical power distribution and variations in 12-channel transmitter module

On the other hand, it was found that ageing has a low impact on the optical output power performance. Fig. 8 hereafter shows an eye-diagram as typically observed at the receiver output after life testing. It is yet well-shaped and perfectly open, indicating that the signal integrity is maintained at up to 10 Gbps and up to 7 Gbps for manufacturer A's and manufacturer B's module, respectively.

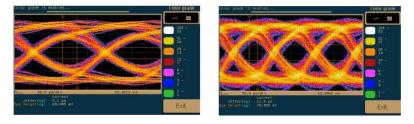


Fig. 8 : Eye diagrams under 10Gbps PRBS modulation (left) manufacturer A and 7Gbps (right) manufacturer B, after 1002 hours after ageing at 125°C

Fig. 9 shows the optical power and eye margin variations during total ionisation dose (TID) testing for one the module. After TID and after an accumulative total dose in proton irradiation of 1×10^{12} p/cm², all tested samples

did not show any significant degradation and their performance remained within specifications. The current consumption did not show major deviation from initial values. No error during BER measurement was found after a rate $> 10^{11}$ bits and transmitter optical output trend over radiation steps showed almost no degradation.

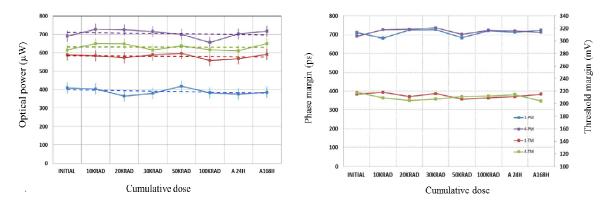


Fig. 9 : Optical power (left) and eye margin (right) variations during TID testing the optoelectronic module

Similarly, radiation testing showed that no optical loss variation higher than 0.5dB appeared in any splitter, and no radiation-dose dependent effect was identified as illustrated in Fig. 10.

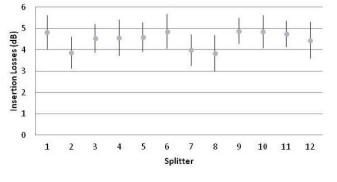


Fig. 10 : Insertion loss of the passive module after TID testing

V. INTEGRATION AND TEST OF THE OPTICAL INTERCONNECT BREADBOARD

Each slice of the demonstrator was stacked and screwed to its neighbour, until the ten slices were attached together so as to achieve a solid mechanical structure. The optical interconnect plane was mounted on top of it, first in vertical position to facilitate the insertion of the MPO multi-fibre connectors in their adapters, and then once the connections were finished, placed in horizontal position as shown in Fig. 11. Most of the fibres inside the optical flex were used to interconnect transmitter to receiver ends through multi-fibre connectors. Some other fibres enabled the signals to pass through the optical coupler module, and the others interconnect transmitter or receiver to the external multi-fibre connector ends.



Fig. 11 : Interconnects of the optical plane to different slices of the breadboard

The test set-up made use of a FPGA breadboard to feed the demonstrator with high-speed binary sequences and measure the BER and eye diagram openings. The Rocket I/O breadboard delivered a 6.5 Gbps data rate signal

to the transmitter module. Electrical signals recovered at the output of the receiver modules were fed back to the FPGA breadboard to calculate a BER after more than 10^{12} sent bit, or sent to an oscilloscope to draw an eye diagram. Measurements were all done using the same bias and modulation current settings for all the transmitter lasers.

The entire optical interconnect breadboard was arranged in different configurations for testing in functional and environmental conditions (thermal vacuum and after vibrations). In particular, the following configurations were used:

- Direct interconnects from Tx/Rx slice to Tx/Rx slice,
- Interconnects from Tx/Rx slice to Tx/Rx slice through external connectors,
- Interconnects from Tx/Rx slice to Tx/Rx slice through optical couplers and through couplers and external connectors,
- Optical interconnect losses were also evaluated.

All these tests were performed at ambient temperature and at atmospheric pressure.



Fig. 12 : Optical interconnect breadboard under environmental test: thermal vacuum (left) and vibrations (right)

The demonstrator was tested in thermal vacuum chamber, and also in thermal chamber at atmospheric pressure at 25° C, $+70^{\circ}$ C and at -30° C as illustrated in Fig. 12. In thermal vacuum conditions, the tested configurations were the same as for functional testing, but with less channels under test due to limited availability of I/O at hermetic feed-through. The optical flex and connector losses were not evaluated during that test for the same reason. Vibration testing was achieved by applying the same test conditions as for qualification of a digital processor EQM.

Fig. 13 and Fig. 14 hereafter show some examples of the eye diagram measured in different configurations. BER testing and eye diagram showed better performance for manufacturer A's module than for manufacturer's B modules. On the other hand, manufacturer B's modules were found to deliver higher optical output power than manufacturer A's modules.

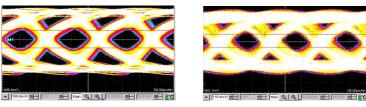


Fig. 13 : Eye diagram at 70°c in thermal chamber: manufacturer A (left) and B (right)

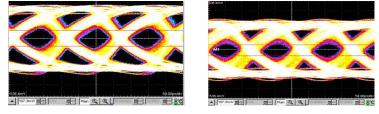


Fig. 14 : Eye diagram at 25°c after vibration: manufacturer A (left) and B (right)

In thermal vacuum chamber, all tested links were working well at hot, ambient and low temperatures but the BER target of less than 10^{-12} was achieved only at 3.25 Gbps for the modules from both manufacturers. At 6.5 Gbps, the performance was impaired by electrical disturbances in the test bench itself and in the long cables (4

meters in and 4 meters out) used to interconnect the breadboard.

In the thermal chamber, the results were found to be better, as expected considering that electrical disturbances from the test bench itself were lower (2-meter cables instead of 4-meter cables). The BER target of 10^{-12} was achieved at 6.5 Gbps for the module from manufacturer A at hot and ambient temperatures, and at 5.2 Gbps for the module from manufacturer B. At cold temperature, the BER target was achieved at up to 3.25 Gbps with both modules.

After vibrations, all the tested links were working nominally at 25° C, proving that the solutions developed for mounting are compatible with space mechanical environment. The BER target of 10^{-12} was achieved at up to 6.5 Gbps for the all the channels of manufacturer A's module, and most of the channels of manufacturer B's module.

The optical interconnect losses did not show any deviation from the initial measurement larger than 0.8 dB.

VI. CONCLUSIONS

A high-throughput optical interconnect breadboard demonstrator was designed and assembled making use of the mechanical structure of the last-generation DTP, and integrating key optoelectronic and optical components developed within the project, namely multi-channel transceivers, transmitters and receivers, optical couplers and fibre circuits. 12-channel transmitter and receiver as well as 4-channel transceiver modules operating at up to 10Gbps line rate were successfully manufactured and tested, thus supporting an aggregate rate in the 50-120 Gigabit/s range. A flexible optical circuit was used to route fibres from board to board, and link transmitter to receiver ends through multi-fibre connectors. This optical interconnect solution is scalable to one thousand optical fibre links and to an overall throughput in excess of 1 Terabit/s.

These components as well as the entire optical interconnect breadboard were tested in both functional and environmental aspects. The functional and thermal testing showed that the performance of the optoelectronic modules from both manufacturers were compliant with, or very close to, the target specifications. On the other hand, some spreading in performance was observed between modules and from channel to channel. This could be improved by setting the bias and modulation currents specifically for each channel, based on preliminary laser testing. No further degradation was observed during the testing after vibration, proving that the optical interconnect breadboard was quite robust.

In summary, the demonstrator was shown to successfully pass the whole environmental testing campaign, thus increasing the technology readiness level and bringing higher confidence in the introduction of optical interconnect technology in future, highly-demanding on-board digital processors.

ACKNOWLEDGEMENTS

This work was carried out in the frame of the ESTEC contract N° 22018/08/NL/NA *Optical Inter-board Interconnects for High Throughput on-Board Processors (OI2)*. The authors acknowledge support from ESA, the European Space Agency, from CNES, the French National Space Agency, as well as from the Finish and Spanish national space agencies. The authors also thank Nikos Karafolas as a Technical Officer for having initiated this activity and stimulated and advised their work all along the project.

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