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The APS+ and intelligent active pixel sensor centered on low power

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The APS+ an intelligent active pixel sensor centered on low power.

Ning Xie¹, Albert Theuwissen^{1,2}, Bernhard Büttgen¹
Henk Hakkesteegt³, Henk Jansen³, Johan Leijtens³

1.Delft University of Technology, Delft, The Netherlands
2.Harvest Imaging, Bree, Belgium
3.TNO, Delft, The Netherlands

Project introduction

Micro-Digital Sun Sensor (μ DSS)

Project introduction (cont.)

Micro-Digital Sun Sensor ($\square$ DSS)

- CMOS image sensor array
- Pin Hole aperture
- $\theta = +47^\circ \dots -47^\circ$: sunlight incident angle
- Accuracy depends on:
 - Centroiding accuracy
 - Height of membrane
 - Straylight properties

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Chip architecture

- APS: Image sensor (3 metal)
- Algorithm Circuit (4 metal)
- ADC (4 metal)
- TXD: serial output signal
- SEL free by design

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Chip architecture (cont.)

- 5*5mm² chip
- TSMC 0.18μm CMOS Image Sensor (CIS) process
- Multi project wafer

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Measurement results

Sun sensor used as a conventional image sensor

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Noise reduction through “Quadra Sample Method”

Conventional sampling (1):
Sample3 (reset noise)

Conventional sampling (2):
CDS: Sample2 – Sample3 (1/f noise)

$$(\text{Sample4} - \text{Sample3}) - (\text{Sample1} - \text{Sample2})$$

(1/f noise canceled)
(reset noise canceled)
reset noise & 1/f noise free

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Row and Column profiling

• Acquisition mode (coarse location, 368x368 pixels)
“Winner Takes It All”

- Column profiling
- Row profiling

ROI is determined fast

• Tracking mode (fine location, 21x21 pixels)

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Measurement results

Sun sensor in acquisition mode

- Peaks of column and row profiling indicate the location of the sun spot
- ROI is defined

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Row and column profiling details

“Winner Takes It All” Principle

- (1) RST are active, $V1=V2=V3=VDD$, V_c is high
- (2) $RS<1:3>$ are active, $V_c=VDD+V_{th}$
- (3) After integration, assuming 2nd pixel is the most illuminated, $V2<V1<V3$, V_c still high
- (4) $RS<1:3>$ are active, $V_c=V2+V_{th}$

V_c follows $V2$ (“Winner”)

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Low power and balanced

- 21.34 mW acquisition mode measured
- 21.40 mW tracking mode measured
- 11 mW for ADC

harvest
imaging

ADC design copied from DALSA imager

- 12-bit pipeline ADC;
- Implemented in TSMC 0.18 process, 4 metal ;
- Sensor output swing: 0.6V, $V_{CM}=2.13V$, conversion rate: 1MSPS

Parameter	Symbol	Min	Nom	Max	Unit
Power Supply	VDDD	3.0	3.3	3.6	V
Input Capacitance	Cin		1.6		pF
Single-ended input swing	Vrange	0.7	1.3	1.5	V
Common mode input range	V _{CM}	0.8		2.3	V
Conversion Rate	F _{SAMP}			60	MSPS
Latency	tl		13		clock cycles
Resolution	N		12		bits

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Conclusion

- ◆ APS+ is highly integrated and power efficient
- ◆ Low noise due to quadra sampling (0.004 degrees measured for $\pm 47^\circ$ sensor)
- ◆ Highly specialized in centroïding
- ◆ Balanced power consumption in both modes of operation

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centered on low power

Thank you!

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