Front Matter: Volume 6520
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Please use the following format to cite material from this book:


ISSN 0277-786X
ISBN 9780819466396

Published by
SPIE—The International Society for Optical Engineering
P.O. Box 10, Bellingham, Washington 98227-0010 USA
Telephone 1 360/676-3290 (Pacific Time) · Fax 1 360/647-1445
http://www.spie.org

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Printed in the United States of America.
# Contents

**Part One**

| xxv | Lithography beyond 32-nm: a role for imprint? (Plenary Paper)  
| M. Melliar-Smith, Molecular Imprints (USA) |

## SESSION 1  PAST, PRESENT, AND FUTURE DIRECTIONS

| 652002 | Marching of the microlithography horses: electron, ion, and photon — past, present, and future (Invited Paper)  
| B. J. Lin, Taiwan Semiconductor Manufacturing Co., Inc. (Taiwan) |

| 652003 | Future directions for CMOS device technology development from a system application perspective (Invited Paper)  
| T. H. Ning, IBM Thomas J. Watson Research Ctr. (USA) |

| 652004 | Optical lithography: 40 years and holding (Invited Paper)  
| J. H. Bruning, Corning Tropel Corp. (USA) |

## SESSION 2  IMMERSION STATUS AND PERFORMANCE

| 652005 | Defects, overlay, and focus performance improvements with five generations of immersion exposure systems (Invited Paper)  

| 652006 | Current status of high-index immersion lithography development (Invited Paper)  

---

**Pagination:** Proceedings of SPIE follow an e-First publication model, with papers published first online and then in print and on CD-ROM. Papers are published as they are submitted and meet publication criteria. A unique, consistent, permanent citation identifier (CID) number is assigned to each article at the time of the first publication. Utilization of CIDs allows articles to be fully citable as soon they are published online, and connects the same identifier to all online, print, and electronic versions of the publication.

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- The first four digits correspond to the SPIE volume number.
- The last two digits indicate publication order within the volume using a Base 36 numbering system employing both numerals and letters. These two-number sets start with 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B ... 0Z, followed by 10-1Z, 20-2Z, etc.

The CID number appears on each page of the manuscript. The complete citation is used on the first page, and an abbreviated version on subsequent pages.
652007 Integrating immersion lithography in 45-nm logic manufacturing [6520-07]
M. Benndorf, NXP Semiconductors (France); S. Warrick, W. Conley, D. Cruau, Freescale Semiconductors, Inc. (France); D. DeSimone, K. Mestadi, V. Farys, ST Microelectronics (France); J.-W. Gemmink, NXP Semiconductors (France)

652008 Performance of immersion lithography for 45-nm-node CMOS and ultra-high density SRAM with 0.25um² [6520-08]
S. Mimotogi, Toshiba Corp. (Japan); F. Uesawa, Sony Corp. (Japan); M. Tominaga, NEC Electronics Corp. (Japan); H. Fujise, K. Sho, Toshiba Corp. (Japan); M. Katsumata, H. Hane, A. Ikeyami, Sony Corp. (Japan); S. Nagahara, NEC Electronics (Japan); T. Ema, M. Asano, H. Kanai, T. Kimura, S.-C. Moon, J.-W. Kim, Hynix Semiconductor Inc. (South Korea)

652009 Benefit of ArF immersion lithography in 55 nm logic device manufacturing [6520-09]
T. Uchiyama, T. Tamura, K. Yoshimochi, NEC Electronics Corp. (Japan); P. Graupner, Carl Zeiss, Semiconductor Manufacturing Technology AG (Germany); H. Bakker, E. van Setten, ASML (Netherlands); K. Morisaki, ASML Japan (Japan)

SESSION 3 HYPER-NA AND POLARIZATION

65200A Snell or Fresnel: the influence of material index on hyper-NA lithography (Invited Paper) [6520-10]
B. Smith, J. Zhou, Rochester Institute of Technology (USA)

65200B Hyper NA polarized imaging of 45-nm DRAM [6520-11]
C.-M. Lim, S. Park, Y.-S. Hyun, J.-S. Kim, T.-S. Eom, J.-T. Park, S.-C. moon, J.-W. Kim, Hynix Semiconductor Inc. (South Korea)

65200C Pushing the boundary: low-k1 extension by polarized illumination [6520-12]
E. van Setten, W. de Boeij, B. Hepp, N. le Masson, G. Swinkels, M. van de Kerkhof, ASML Netherlands B.V. (Netherlands)

65200D Modeling polarization for hyper-NA lithography tools and masks [6520-13]
K. Lai, IBM SRDC (USA); A. E. Rosenbluth, IBM T. J. Watson Research Ctr. (USA); G. Han, J. Tirapu-Azpiroz, J. Meiring, IBM SRDC (USA); A. Goehnermeier, B. Kneer, M. Totzeck, Carl Zeiss SMT AG (Germany); L. de Winter, W. de Boeij, M. van de Kerkhof, ASML Netherlands B.V. (Netherlands)

65200E Polarization-dependent proximity effects [6520-14]
J. K. Tyminski, Nikon Precision Inc. (USA); T. Matsuura, T. Nakashima, Nikon Corp. (Japan); T. Schmoeller, Synopsys Inc. (Germany); J. Lewellen, Synopsys Inc. (USA)

65200F The impact of projection lens polarization properties on lithographic process at hyper-NA [6520-15]
B. Geh, Carl Zeiss SMT AG (Germany) and ASML US, Inc. (USA); J. Rouff, J. Zimmermann, P. Gräupner, M. Totzeck, M. Mengel, U. Hempelmann, Carl Zeiss SMT AG (Germany); E. Schmitt-Weaver, ASML US, Inc. (USA)
SESSION 4  DOUBLE PATTERNING TECHNOLOGY

65200G  Pitch doubling through dual-patterning lithography challenges in integration and litho budgets [6520-16]
M. Dusa, ASML US Inc. (USA); J. Quaedackers, O. F. A. Larsen, J. Meessen, E. van der Heijden, G. Dicker, O. Wismans, P. de Haas, K. van Ingen Schenau, J. Finders, B. Vleeming, ASML Netherlands B.V. (Netherlands); G. Storms, P. Jaenen, S. Cheng, M. Maenhoudt, IMEC (Belgium)

65200H  Issues and challenges of double patterning lithography in DRAM [6520-17]
S.-M. Kim, S.-Y. Koo, J.-S. Choi, Y.-S. Hwang, J.-W. Park, E.-K. Kang, C.-M. Lim, S.-C. Moon, J.-W. Kim, Hynix Semiconductor Inc. (South Korea)

65200I  Manufacturability issues with double patterning for 50-nm half-pitch single damascene applications using RELACS shrink and corresponding OPC [6520-18]
M. Op de Beeck, J. Versluijs, V. Wiaux, T. Vandeweyer, I. Cloifi, H. Struyf, D. Hendrickx, J. Van Olmen, IMEC (Belgium)

65200J  The modeling of double patterning lithographic processes [6520-19]
S. A. Robertson, T. Graves, M. D. Smith, J. J. Biafore, KLA-Tencor Corp. (USA)

65200K  Dark field double dipole lithography (DDL) for back-end-of-line processes [6520-97]
M. Burkhardt, S. Burns, IBM Research (USA); D. Dunn, IBM SRDC (USA); T. A. Brunner, IBM Research (USA); S. D. Hsu, J. Park, ASML MaskTools Inc. (USA)

SESSION 5  OPTIMIZATION, CONTROL, AND PERFORMANCE

65200L  Evaluating the performance of a 193-nm hyper-NA immersion scanner using scatterometry [6520-21]
O. Kritsun, B. La Fontaine, R. Sandberg, A. Acheta, H. J. Levinson, K. Lensing, Advanced Micro Devices, Inc. (USA); M. Dusa, J. Hauschild, A. Pici, ASML MaskTools Inc. (USA); C. Saravanan, K. Primak, R. Korlahalli, S. Nirmalgandhi, Nanometrics Inc. (USA)

65200M  Distinguishing dose, focus, and blur for lithography characterization and control [6520-22]
C. P. Ausschnitt, T. A. Brunner, IBM Semiconductor Research and Development Ctr. (USA)

65200N  Patterning control budgets for the 32-nm generation incorporating lithography, design, and RET variations [6520-23]
K. Lucas, Synopsys, Inc. (USA); C. Cork, Synopsys SARL (France); J. Cobb, Synopsys, Inc. (USA); B. Ward, Synopsys, Inc. (USA) and IMEC (Belgium); M. Drapeau, Synopsys, Inc. (Canada); C. Zhang, Synopsys, Inc. (USA); J. Allgair, International SEMATECH (USA); M. Kling, M. Rieger, Synopsys, Inc. (USA)

65200O  Control of polarization and apodization with film materials on photomasks and pellicles for high NA imaging performance [6520-24]
W.-H. Cheng, J. Farnsworth, Intel Corp. (USA)

65200P  Global optimization of masks, including film stack design to restore TM contrast in high NA TCCs [6520-25]
A. E. Rosenbluth, D. Melville, IBM T.J. Watson Research Ctr. (USA); K. Tian, K. Lai, N. Seong, IBM Semiconductor Research and Development Ctr. (USA); D. Pfeiffer, M. Colburn, IBM T.J. Watson Research Ctr. (USA)
### SESSION 6  OPC AND ADVANCED MODELING I

**65200Q**  A solution for exposure tool optimization at the 65-nm node and beyond [6520-26]
D. Itai, Canon Inc. (Japan)

**65200R**  Fast and accurate 3D mask model for full-chip OPC and verification [6520-27]
P. Liu, Y. Cao, L. Chen, G. Chen, M. Feng, J. Jiang, H. Liu, Brion Technologies, Inc. (USA); S. Suh, S.-W. Lee, S. Lee, Samsung Electronics, Co. LTD (South Korea)

**65200S**  Process window and interlayer aware OPC for the 32-nm node [6520-28]

**65200T**  OPC in memory-device patterns using boundary layer model for 3-dimensional mask topographic effect [6520-29]
Y.-C. Kim, I. Kim, J. Park, S. Kim, S. Suh, Y. Cheon, S. Lee, J. Lee, C.-J. Kang, J. Moon, Samsung Electronics Co., Ltd. (South Korea); J. Cobb, S. Lee, Synopsys, Inc. (USA)

**65200U**  Generalized inverse lithography methods for phase-shifting mask design [6520-30]
X. Ma, G. R. Arce, Univ. of Delaware (USA)

**65200V**  Visualizing the impact of the illumination distribution upon imaging, and applying the insights gained [6520-118]
S. D. Slonaker, Nikon Precision Inc. (USA)

### SESSION 7  IMAGE QUALITY AND CHARACTERIZATION

**65200X**  Sources and scaling laws for LER and LWR [6520-33]
T. Sandstrom, C. Rydberg, Micronic Laser Systems AB (Sweden)

**65200Y**  Polarization aberration analysis using Pauli-Zernike representation [6520-34]
N. Yamamoto, Spansion Japan Ltd. (Japan); J. Kye, H. J. Levinson, Advanced Micro Devices, Inc. (USA)

**65200Z**  Best focus determination: bridging the gap between optical and physical topography [6520-36]
F. Kahlenberg, R. Seltmann, AMD Fab 36 LLC & Co. KG (Germany); B. M. La Fontaine, AMD Strategic Lithography Technology (USA); R. Wirtz, AMD Saxony LLC & Co. KG (Germany); A. Kisteman, R. N. M. Vanneer, M. Pieters, ASML Netherlands B.V. (Netherlands)

**652011**  Study of iso-dense bias (IDB) sensitivity to laser spectral shape at the 45nm node [6520-138]
K. Yoshimochi, T. Uchiyama, T. Tamura, NEC Electronics Corp. (Japan); T. Theeuwes, R. Peeters, H. van der Laan, H. Bakker, ASML Netherlands B.V. (Netherlands); K. Morisaki, ASML Japan Co., Ltd. (Japan); T. Oga, Cymer Japan, Inc. (Japan)
### SESSION 8  CHALLENGES FOR WATER IMMERSION

**652012** Immersion defect reduction: II. The formation mechanism and reduction of patterned defects [6520-38]

**652013** Optical error sensitivities of immersion lithography [6520-39]
Z. G. Chen, K. Lai, K. Racette, IBM Microelectronics (USA)

**652014** Contamination and particle control system in immersion exposure tool [6520-40]

**652015** Extending immersion lithography to the 32-nm node [6520-41]
S. Warrick, W. Conley, Freescale Semiconductor (France); V. Farys, ST Microelectronics (France); M. Benndorf, J.-W. Gemmink, NXP Semiconductors (France); Y. Trouiller, ST Microelectronics (France); J. Beliedent, NXP Semiconductors (France); D. Jovanovic, Freescale Semiconductor (France); P. Gouraud, ST Microelectronics (France)

**652016** Immersion defectivity study with volume production immersion lithography tool [6520-42]

### SESSION 9  COMPUTATIONAL LITHOGRAPHY: JOINT SESSION WITH CONFERENCE 6521

**652017** Lossless compression algorithm for hierarchical IC layout data [6520-43]
A. Gu, A. Zakhor, Univ. of California, Berkeley (USA)

**652018** Advances in compute hardware platforms for computational lithography [6520-44]
T. Kingsley, J. Sturtevant, Mentor Graphics Corp. (USA); S. McPherson, M. Sexton, Mercury Computer Corp., Inc. (USA)

**652019** SEM image contouring for OPC model calibration and verification [6520-167]
C. Tabery, Advanced Micro Devices, Inc. (USA); H. Morokuma, R. Matsuoka, Hitachi High-Technologies Corp. (Japan); L. Page, Hitachi High Technologies America, Inc. (USA); G. E. Bailey, I. Kusnadi, T. Do, Mentor Graphics Corp. (USA)

### SESSION 10  ADVANCED RESOLUTION ENHANCEMENT

**65201A** Phase-shifted assist feature OPC for sub-45-nm node optical lithography [6520-45]
G.-S. Yoon, H.-B. Kim, J.-W. Lee, S.-W. Choi, W.-S. Han, Samsung Electronics Co., Ltd. (South Korea)

**65201B** The random contact hole solutions for future technology nodes [6520-46]
A. Chen, ASML Taiwan Ltd. (Taiwan); S. Hansen, ASML US, Inc. (USA); M. Moers, ASML Netherlands B.V. (Netherlands); J. Shieh, ASML Taiwan Ltd. (Taiwan); A. Engelen, K. van Ingen Schenau, ASML Netherlands B.V. (Netherlands); S. Tseng, ASML Taiwan Ltd. (Taiwan)
Patterning with amorphous carbon spacer for expanding the resolution limit of current lithography tool [6520-48]
W.-Y. Jung, S.-M. Kim, C.-D. Kim, G.-H. Sim, S.-M. Jeon, S.-W. Park, B.-S. Lee, S.-K. Park, Hynix Semiconductor Inc. (South Korea); J.-S. Kim, L.-S. Heon, Lam Research Corp. (USA)

32-nm SOC printing with double patterning, regular design, and 1.2 NA immersion scanner [6520-49]
Y. Trouiller, LETI-CEA (France); V. Farys, STMicroelectronics (France); A. Borjon, J. Belledent, C. Couderc, Philips Semiconductors (France); F. Sundermann, J.-C. Urbani, STMicroelectronics (France); Y. Rody, Philips Semiconductors (France); C. Gardin, Freescale Semiconductor (France); J. Planchot, STMicroelectronics (France); W. Conley, Freescale Semiconductor (France); P.-J. Gairand, STMicroelectronics (France); S. Warrick, Freescale Semiconductor (France); F. Robert, G. Kerrien, F. Vautrin, STMicroelectronics (France); B. Wilkinson, M. Saied, E. Yesilada, P. Montgomery, Freescale Semiconductor (France); L. Le Cam, Philips Semiconductors (France); C. Martinelli, STMicroelectronics (France)

Ultra-low k1 oxide contact hole formation and metal filling using resist contact hole pattern by double I&F formation method [6520-50]

RET application in 45-nm node and 32-nm node contact hole dry ArF lithography process development [6520-47]

Part Two

SESSION 11 MASK EFFECT AND TECHNOLOGIES

Pupil plane analysis on AIMS 45-193i for advanced photomasks [6520-52]

The impact of the mask stack and its optical parameters on the imaging performance [6520-53]
A. Erdmann, T. Fühner, S. Seifert, S. Popp, P. Evanschitzky, Fraunhofer Institute of Integrated Systems and Device Technology (Germany)

Mask 3D effect on 45-nm imaging using attenuated PSM [6520-54]
K. Sato, M. Itoh, T. Sato, Toshiba Corp. (Japan)

Effects of reticle birefringence on 193-nm lithography [6520-55]
S. Light, I. Tsyba, Micron Technology, Inc. (USA); C. Petz, Univ. of Washington (USA); P. Baluswamy, B. Rolfson, Micron Technology, Inc. (USA)
SESSION 12 IMMERSION ADVANCEMENTS BEYOND WATER

65201L Early look into device level imaging with beyond water immersion [6520-56]
W. Conley, S. Warrick, Freescale Semiconductor, Inc. (France); C. Garza, Freescale Semiconductor, Inc. (USA); P.-J. Goirand, ST Microelectronics (France); J.-W. Gemmink, NXP (France); D. Van Steenwinckel, NXP Research (Belgium)

65201M Extending immersion lithography with high-index materials: results of a feasibility study [6520-57]
H. Sewell, ASML US, Inc. (USA); J. Mulkens, ASML Netherlands B.V. (Netherlands); P. Graepner, Zeiss SMT (Germany); D. McCafferty, L. Markoya, ASML US, Inc. (USA); S. Donders, ASML Netherlands B.V. (Netherlands); N. Samarakone, ASML US, Inc. (USA); R. Duesing, Zeiss SMT AG (Germany)

65201O High-index immersion lithography with second-generation immersion fluids to enable numerical apertures of 1.55 for cost effective 32-nm half pitches [6520-59]
R. H. French, DuPont Co. (USA); V. Liberman, MIT Lincoln Lab (USA); H. V. Tran, J. Feldman, D. J. Adelman, R. C. Wheland, W. Qiu, S. J. McLain, DuPont Co. (USA); O. Nagao, M. Kaku, DuPont K. K. (Japan); M. Mocella, M. K. Yang, M. F. Lemon, L. Brubaker, A. L. Shoe, B. Fones, B. E. Fischel, DuPont Co. (USA); K. Krohn, D. Hardy, MIT Lincoln Lab (USA); C. Y. Chen, DuPont-EKC (USA)

65201P High-index fluoride materials for 193-nm immersion lithography [6520-60]
T. Nawata, Y. Inui, I. Masada, E. Nishijima, T. Mabuchi, N. Mochizuki, Tokuyama Corp. (Japan); H. Satoh, T. Fukuda, Tohoku Univ. (Japan)

65201Q Feasibility of 37-nm half-pitch with ArF high-index immersion lithography [6520-61]
Y. Sekine, M. Kawashima, E. Sakamoto, K. Sakai, A. Yamada, T. Honda, Canon Inc. (Japan)

SESSION 13 OPC AND ADVANCED MODELING II

65201R Application of full-chip optical proximity correction for sub-60-nm memory device in polarized illumination [6520-62]
H.-S. Yune, Y.-B. Ahn, D. Lee, J. Moon, B.-H. Nam, D. Yim, Hynix Semiconductor Inc. (South Korea)

65201S Utilization of optical proximity effects for resist image stitching [6520-63]
Y. Fan, T. Castro, Intel Corp. (USA)

65201T Methods for comparative extraction of OPC response [6520-64]
T. E. Zavecz, TEA Systems (USA)

65201U ACLV driven double-patterning decomposition with extensively added printing assist features (PrAFs) [6520-65]
J. E. Meiring, IBM SRDC (USA); H. Haffner, Infineon Technologies NA Corp. (USA); C. Fonseca, S. D. Halle, S. M. Mansfield, IBM SRDC (USA)

65201V A discussion of the regression of physical parameters for photolithographic process models [6520-66]
L. S. Melvin III, K. D. Lucas, Synopsys, Inc. (USA)
SESSION 14  ADVANCED EXPOSURE SYSTEMS AND COMPONENTS I

65201W  Latest results from the hyper-NA immersion scanners S609B and S610C [6520-67]
J. Ishikawa, T. Fujiwara, K. Shiraishi, Y. Ishii, M. Nei, Nikon Corp. (Japan)

65201X  Immersion exposure tool for the 45-nm HP mass production [6520-68]
H. Kubo, H. Hata, F. Sakai, N. Deguchi, T. Iwanaga, T. Ebihara, Canon Inc. (Japan)

65201Y  Performance of a 1.35NA ArF immersion lithography system for 40-nm applications [6520-69]
J. de Klerk, C. Wagner, R. Droste, L. Levasier, L. Jorritsma, E. van Setten, H. Kattouw,
J. Jacobs, ASML Netherlands B.V. (Netherlands); T. Heil, Carl Zeiss SMT AG (Germany)

65201Z  Exposure and compositional factors that influence polarization induced birefringence in silica glass [6520-70]
D. C. Allan, M. Mlejnek, U. Neukirch, C. M. Smith, F. M. Smith, Corning Inc. (USA)

652020  XLR 500i: recirculating ring ArF light source for immersion lithography [6520-71]
D. W. Brown, P. O’Keeffe, V. B. Fleurov, R. Rokitski, R. Bergstedt, I. V. Fomenkov, K. O’Brien,
N. R. Farrar, W. N. Partlo, Cymer Inc. (USA)

SESSION 15  ADVANCED EXPOSURE SYSTEMS AND COMPONENTS II

652021  Catadioptric projection lens for 1.3 NA scanner [6520-72]
T. Matsuyama, Y. Ohmura, Y. Fujishima, T. Koyama, Nikon Corp. (Japan)

652022  New projection optics and aberration control system for the 45-nm node [6520-73]
T. Yoshihara, B. Takeshita, A. Shigenobu, Y. Hasegawa, Y. Ohsaki, K. Mishima, S. Miura,
Canon Inc. (Japan)

652023  Integration of a new alignment sensor for advanced technology nodes [6520-74]
P. Hinnen, ASML Netherlands B.V. (Netherlands); J. Depre, S. Tanaka, ASML Japan Co., Ltd.
(Japan); S.-Y. Lim, O. Brioso, M. Shahjerdy, ASML Netherlands B.V. (Netherlands); K. Ishigo,
T. Kono, T. Higashi, Toshiba Corp. (Japan)

652024  Ultra line narrowed injection lock laser light source for higher NA ArF immersion lithography tool [6520-75]
T. Suzuki, Komatsu Ltd. (Japan); K. Kakizaki, Ushio Inc. (Japan); T. Matsunaga, Komatsu Ltd.
(Japan); S. Tanaka, Ushio Inc. (Japan); Y. Kawanishi, Komatsu Ltd. (Japan); M. Shimbori,
M. Yoshino, Ushio Inc. (Japan); T. Kumazaki, H. Umeda, Komatsu Ltd. (Japan); H. Nagano,
Ushio Inc. (Japan); S. Nagai, Komatsu Ltd. (Japan); Y. Sasaki, Ushio Inc. (Japan); H. Mizoguchi,
Gigaphoton Inc. (Japan)

652025  Demonstration of sub-45-nm features using azimuthal polarization on a 1.30NA immersion microstepper [6520-77]
E. C. Piscani, SEMATECH, Inc. (USA); S. Palmer, Texas Instruments (USA) and SEMATECH, Inc.
(USA); C. Van Peski, SEMATECH, Inc. (USA)
### POSTER SESSION: DEVELOPMENTS IN RET

<table>
<thead>
<tr>
<th>Session</th>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>652026</td>
<td>Optical performance enhancement technique for 45-nm-node with binary mask</td>
<td>J.-S. Jung, H.-B. Kim, J.-W. Lee, S.-W. Choi, W.-S. Han, Samsung Electronics Co., Ltd. (South Korea)</td>
</tr>
<tr>
<td>652029</td>
<td>Process window optimization of CPL mask for beyond 45-nm lithography</td>
<td>S. Y. Tan, Q. Lin, Chartered Semiconductor Manufacturing Ltd. (Singapore); C. J. Tay, C. Quan, National Univ. of Singapore (Singapore)</td>
</tr>
<tr>
<td>65202A</td>
<td>SRAF placement and sizing using inverse lithography technology</td>
<td>T. Lin, Luminescent Technologies, Inc. (USA); F. Robert, A. Borjon, Crolles II Alliance (France); G. Russell, Luminescent Technologies, Inc. (USA); C. Martinelli, Crolles II Alliance (France); A. Moore, Luminescent Technologies, Inc. (USA); Y. Rody, Crolles II Alliance (France)</td>
</tr>
<tr>
<td>65202B</td>
<td>Optimal SRAF placement for process window enhancement in 65-nm/45-nm technology</td>
<td>C. Sarma, K. Herold, Infineon Technologies NA (USA); C. Noelscher, Qimonda Dresden GmbH &amp; Co OHG (Germany); P. Schroeder, Infineon Technologies NA (USA)</td>
</tr>
<tr>
<td>65202C</td>
<td>Intensity weighed focus drilling exposure for maximizing process window of sub-100-nm contact by simulation</td>
<td>S. Jung, T.-C. Yang, T.-H. Yang, K.-C. Chen, C.-Y. Lu, Macronix International Co., Ltd. (Taiwan)</td>
</tr>
<tr>
<td>65202D</td>
<td>Process margin improvement using custom transmission EAPSM reticles</td>
<td>J. Buntin, S. Agarwal, B. Rolfson, R. Housley, B. Baggenstoss, E. Byers, Micron Technology Inc. (USA); C. Progler, Photronics, Inc. (USA)</td>
</tr>
<tr>
<td>65202E</td>
<td>Verification of high-transmittance PSM with polarization at 193-nm high-NA system</td>
<td>C. F. Chiu, C. L. Chen, J. W. Lee, W. B. Wu, C. L. Shih, F. Y. Chen, J. P. Lin, NANYA Technology Corp. (Taiwan)</td>
</tr>
</tbody>
</table>

### POSTER SESSION: DOUBLE PATTERNING AND EXPOSURE TECHNOLOGY

<table>
<thead>
<tr>
<th>Session</th>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
<tbody>
<tr>
<td>65202F</td>
<td>A litho-only approach to double patterning</td>
<td>A. Vanleenhove, D. Van Steenwinckel, NXP Semiconductors (Belgium)</td>
</tr>
<tr>
<td>65202H</td>
<td>A study of double exposure process design with balanced performance parameters for line/space applications</td>
<td>J. Zhu, Shanghai IC R&amp;D Ctr. (China); P. Wu, Q. Wu, H. Ding, X. Li, C. Sun, NEC Electronics Co., Ltd. (China)</td>
</tr>
</tbody>
</table>
The improvement of photolithographic fidelity of two-dimensional structures through double exposure method [6520-91]
Q. Wenren, H. Ding, X. Li, C. Sun, Shanghai Huahong NEC Electronics Co., Ltd. (China); J. Zhu, Shanghai Integrated Circuit Research and Development Ctr. (China); Q. Wu, Shanghai Huahong NEC Electronics Co., Ltd. (China)

Double patterning with multilayer hard mask shrinkage for sub-0.25 k1 lithography [6520-92]

Sub-k1 = 0.25 lithography with double patterning technique for 45-nm technology node flash memory devices at λ = 193nm [6520-93]
G. Capetti, P. Cantù, E. Galassini, A. Vaglio Pret, C. Turco, A. Vaccaro, P. Rigolli, F. D'Angelo, G. Cotti, STMicroelectronics (Italy)

Quantum state control interference lithography and trim double patterning for 32-16 nm lithography [6520-94]
R. D. Frankel, B. W. Smith, A. Estroff, Rochester Institute of Technology (USA)

Double exposure using 193-nm negative tone photoresist [6520-95]
R. Kim, T. Wallow, J. Kye, H. J. Levinson, Advanced Micro Devices, Inc. (USA); D. White, TOK America, Inc. (USA)

Feasibility study of splitting pitch technology on 45-nm contact patterning with 0.93 NA [6520-96]
Y. F. Cheng, Y. L. Chou, T. C. Tseng, B. Y. Hsueh, C. H. Yang, United Microelectronics Corp. (Taiwan)

A study of process window capabilities for two-dimensional structures under double exposure condition [6520-98]
Q. Wu, P. Wu, Shanghai Huahong NEC Electronics Co., Ltd. (China); J. Zhu, Shanghai Integrated Circuit Research and Development Ctr. (China); H. Ding, X. Li, C. Sun, C. Peng, Shanghai Huahong NEC Electronics Co., Ltd. (China)

New double exposure technique without alternating phase-shift mask [6520-99]
T. Yamamoto, T. Yao, H. Futatsuya, T. Chijimatsu, S. Asai, Fujitsu Ltd. (Japan)

ILT for double exposure lithography with conventional and novel materials [6520-100]
A. Poonawala, Univ. of California/Santa Cruz (USA); Y. Borodovsky, Intel Corp. (USA); P. Milanfar, Univ. of California/Santa Cruz (USA)

POSTER SESSION: EXPOSURE TOOLS, SUBSYSTEMS, AND MATERIALS

Development and characterization of a 300-mm dual-side alignment stepper [6520-101]
W. W. Flack, E. M. True, R. Hsieh, D. Fuchs, R. Ellis, Ultratech, Inc. (USA)

Flare effect of different shape of illumination apertures in 193-nm optical lithography system [6520-103]
Y.-J. Yun, J. Kim, K. Kim, Dongbu Electronics Co., Ltd. (South Korea)
Part Three

65202U Silicon verification of flare model and application to real chip for long range proximity correction [6520-104]
D. Zhang, B. I. Choi, F. Y. Mei, S. T. Mulia, J. Y. Hsieh, Chartered Semiconductor Manufacturing Ltd. (Singapore); J. Word, Mentor Graphics Corp. (USA); Y. Yudhistira, Chartered Semiconductor Manufacturing Ltd. (Singapore)

65202V Thermal aberration control for low-k1 lithography [6520-105]
Y. Uehara, T. Matsuyama, T. Nakashima, Y. Ohmura, T. Ogata, K. Suzuki, N. Tokuda, Nikon Corp. (Japan)

65202W Quasi-telecentricity: the effects of unbalanced multipole illumination [6520-106]
S. P. Renwick, Nikon Precision, Inc. (USA)

65202X Novel high-throughput micro-optical beam shapers reduce the complexity of macro-optics in hyper-NA illumination systems [6520-107]
T. Bizjak, T. Mitra, L. Aschke, LiMO Lissotschenko Mikrooptik GmbH (Germany)

65202Z A solid-state 193-nm laser with high spatial coherence for sub-40-nm interferometric immersion lithography [6520-109]
A. J. Merriam, Actinix (USA); D. S. Bethune, J. A. Hoffnagle, W. D. Hinsberg, C. M. Jefferson, IBM Almaden Research Ctr. (USA); J. J. Jacob, Actinix (USA); T. Litvin, Kimokeo, Inc. (USA)

652030 Investigations regarding the prevention of depolarization of ArF excimer laser irradiation by CaF2 laser optics [6520-110]
U. Natura, D. Keutel, M. Letz, L. Parthier, K. Knapp, SCHOTT AG (Germany)

652031 Reliable high-power injection locked 6kHz 60W laser for ArF immersion lithography [6520-111]
H. Watanabe, S. Komae, Gigaphoton Inc. (Japan); S. Tanaka, Ushio Inc. (Japan); R. Nohdami, T. Yamazaki, H. Nakarai, J. Fujimoto, Gigaphoton Inc. (Japan); T. Matsunaga, Komatsu Ltd. (Japan); T. Saito, Gigaphoton inc. (Japan); K. Kakizaki, Ushio Inc. (Japan); H. Mizoguchi, Gigaphoton Inc. (Japan)

652032 Increased availability of lithography light sources using advanced gas management [6520-112]
W. J. Dunstan, R. Jacques, K. O’Brien, A. Ratnam, Cymer, Inc. (USA)

652033 A study of overlay mark robustness and enhanced alignment techniques for alignment improvement on metal layers of sub-100-nm technology [6520-114]
K. Dubey, T. Nakamura, Canon Singapore Pte., Ltd. (Singapore); H. Tanaka, N. Hayashi, S. Egashira, K. Mishima, T. Mase, T. Takeuchi, A. Honda, T. Kakizaki, Canon Inc. (Japan)

652034 The optimization of zero-spaced microlenses for 2.2um pixel CMOS image sensor [6520-115]
H. Nam, J. L. Park, J. S. Choi, J. G. Lee, MagnaChip Semiconductor Inc. (South Korea)
Laser durability studies of high index immersion fluids: fluid degradation and optics contamination effects [6520-197]
V. Liberman, M. Rothschild, S. T. Palmacci, Lincoln Lab., Massachusetts Institute of Technology (USA); P. A. Zimmerman, A. Grenville, Intel Corp./International SEMATECH (USA)

POSTER SESSION: ILLUMINATION OPTIMIZATION AND CONTROL

Illumination optimization with actual information of exposure tool and resist process [6520-116]
K. Tsujita, K. Mikami, R. Naka, N. Baba, T. Ono, A. Suzuki, Canon Inc. (Japan)

Impact of illumination performance on hyper-NA imaging for 45-nm node [6520-117]
K.I. Mori, A. Yamada, T. Shiozawa, K. Takahashi, Canon Inc. (Japan)

Optimal solutions for the illuminator and final lens pupil coupled distributions beyond the axial symmetry [6520-120]
I. Ivonin, T. Sandstrom, Micronic Laser Systems AB (Sweden)

Sensitivity of hyper-NA immersion lithography to illuminator imperfections [6520-122]
W. Gao, SYNOPSYS, Inc. (Germany); L. De Winter, ASML Netherlands B.V. (Netherlands)

POSTER SESSION: IMAGE AND PROCESS MODELING

The calibration of process window model for 55-nm node [6520-123]
T. H. Wu, S. Y. Huang, C. W. Huang, P. R. Tsai, C. H. Yang, United Microelectronics Corp. (Taiwan); I. Y.-J. Su, Synopsys, Inc. (Taiwan); B. Falch, Synopsys, Inc. (USA)

SEM based data extraction for model calibration [6520-124]
M. Al-Imam, H. Y. Liao, J. Schacht, G. E. Bailey, Mentor Graphics Corp. (USA); T. H. Wu, C. W. Huang, S. Y. Huang, P. R. Tsai, C. H. Yang, United Microelectronics Corp. (Taiwan)

Distributed model calibration using Levenberg-Marquardt algorithm [6520-125]
M. Lu, L. Zhu, Grace Semiconductor Manufacturing Corp. (China); L. Ling, G. Zhang, Anchor Semiconductor Inc. (China); W. Chan, X. Zhou, Anchor Semiconductor Inc. (USA)

Analytical approach to high-NA images [6520-126]
S.-K. Kim, Catholic Univ. of Korea (South Korea) and Hanyang Univ. (South Korea)

Modeling and performance metrics for longitudinal chromatic aberrations, focus-drilling, and Z-noise: exploring excimer laser pulse-spectra [6520-127]
M. Smith, KLA-Tencor Corp. (USA); J. Bendik, Dynamic Intelligence Inc. (USA); I. Lalovic, N. Farrar, Cymer, Inc. (USA); W. Howard, C. Sallee, KLA-Tencor Corp. (USA)

Dr.LITHO: a development and research lithography simulator [6520-131]
T. Fühner, T. Schnattinger, G. Ardelean, A. Erdmann, Fraunhofer Institute of Integrated Systems and Device Technology (Germany)

Lithographic characterization of evanescent-wave imaging systems [6520-132]
T. Graves, M. D. Smith, S. A. Robertson, KLA-Tencor Corp. (USA)
Heuristics for truncating the number of optical kernels in Hopkins image calculations for model-based OPC treatment [6520-134]
C. Zuniga, E. Tejinil, ASML Mask Tools Inc. (USA)

POSTER SESSION: IMAGE QUALITY AND CHARACTERIZATION

Topography induced defocus with a scanning exposure system [6520-136]
B. R. Liegl, IBM Microelectronics (USA); N. Felix, Cornell Univ. (USA); C. Brodsky, D. Dobuzinsky, IBM Microelectronics (USA)

Precise measurement of process bias and its relation to MEEF [6520-139]
T. E. Zavecz, TEA Systems Corp. (USA)

Assessment of trade-off between resist resolution and sensitivity for optimization of hyper-NA immersion lithography [6520-140]
Y. Kishikawa, M. Kawashima, A. Ohkubo, Y. Iwasaki, S. Takeuchi, M. Yoshii, T. Honda, Canon Inc. (Japan)

Understanding the impact of rigorous mask effects in the presence of empirical process models used in optical proximity correction (OPC) [6520-141]
M. C. Lam, K. Adam, Mentor Graphics Corp. (USA)

Transistor-based electrical test structures for lithography and process characterization [6520-142]
W. J. Poppe, J. Holwill, L.-T. Pang, P. Friedberg, Q. Liu, L. Alarcon, A. Neureuther, Univ. of California/Berkeley (USA)

Use of starburst patterns in optical lithography [6520-143]
M. Burkhardt, IBM Research (USA); C. Tabery, Advanced Micro Devices Corp. (USA)

Challenging to meet 1-nm iso-dense bias (IDB) by controlling laser spectrum [6520-144]
T. Oga, Cymer, Inc. (Japan); T. Yamamoto, T. Yao, S. Asai, Fujitsu Limited (Japan); T. Kudo, T. Toki, Nikon Corp. (Japan)

Impact of mask error on OPC for 45-nm node [6520-145]
O. Park, Infineon Technologies NA (USA)

Taking image quality factor into the OPC model tuning flow [6520-147]
C.-H. Wang, Q. Liu, Semiconductor Manufacturing International Corp. (China); L. Zhang, Mentor Graphics Corp. (China)

Effects of laser bandwidth on iso-dense bias and line-end shortening at sub-micron process nodes [6520-148]
R. C. Peng, A. K. Yang, L. J. Chen, Y. W. Guo, H. H. Liu, J. Lin, TSMC Corp. (Taiwan); A. Chang, Cymer, Inc. (Taiwan)

On the quality of measured optical aberration coefficients using phase wheel monitor [6520-149]
L. V. Zavyalova, A. R. Robinson, A. Baurov, N. V. Lafferty, B. W. Smith, Rochester Institute of Technology (USA)
A comparative study for mask defect tolerance on phase and transmission for dry and immersion 193-nm lithography [6520-150]
M. L. Ling, National Univ. of Singapore (Singapore); G. S. Chua, Chartered Semiconductor Manufacturing Ltd. (Singapore); C. J. Tay, C. Quan, National Univ. of Singapore (Singapore); Q. Lin, Chartered Semiconductor Manufacturing Ltd. (Singapore)

The causes of horizontal-vertical (H-V) bias in optical lithography: dipole source errors [6520-151]
J. J. Biafore, KLA-Tencor Corp. (USA); C. A. Mack, Lithoguru.com (USA); S. A. Robertson, M. D. Smith, S. Kapasi, KLA-Tencor Corp. (USA)

POSTER SESSION: OPC AND IMPLEMENTATION

OPC-free on-grid fine random hole pattern formation utilizing double resist patterning with double RETs [6520-153]

Virtual OPC at hyper NA lithography [6520-155]
S. Lee, S.-W. Kim, Y.-J. Chun, S.-S. Suh, Y.-K. Jang, S.-J. Lee, S.-W. Choi, W.-S. Han, Samsung Electronics Co., Ltd. (South Korea)

Mask-friendly OPC for a reduced mask cost and writing time [6520-156]
A. Yehia, Mentor Graphics Corp. (USA)

Methods and factors to optimize OPC run-time [6520-157]
A. D. Dave, C. P. Babcock, S. N. McGowan, Y. Zou, Advanced Micro Devices, Inc. (USA)

Golden curve method for OPC signature stability control in high MEEF applications [6520-158]
K. Geidel, Advanced Mask Technology Ctr. GmbH and Co. KG (Germany); T. Franke, Qimonda AG (Germany); S. Roling, AMD Fab 36 LLC and Co. KG (Germany); P. Buck, Toppan Photomasks, Inc. (USA); M. Sczyrba, Advanced Mask Technology Ctr. GmbH and Co. KG (Germany); E. Mittermeier, Qimonda AG (Germany); R. Cinque, Advanced Mask Technology Ctr. GmbH and Co. KG (Germany)

Mask enhancement using an evanescent wave effect (Best Student Paper Award) [6520-159]
N. V. Lafferty, J. Zhou, B. W. Smith, Rochester Institute of Technology (USA)

The gate CD uniformity improvement by the layout retarget with refer to the litho process [6520-160]

Toward standard process models for OPC [6520-161]
Y. Granik, D. Medvedev, N. Cobb, Mentor Graphics Corp. (USA)

Modular process modeling for OPC [6520-162]
M. C. Keck, C. Bodendorf, T. Schmidtfing, Qimonda AG (Germany); R. Schliefl, Qimonda NA (USA); R. Wildfeuer, S. Zumpe, Qimonda GmbH and Co. OHG (Germany); M. Niehoff, Mentor Graphics Corp. (Germany)
**POSTER SESSION: OPTIMIZATION, CONTROL, AND PERFORMANCE**

65204G  **Fast predictive post-OPC contact/via printability metric and validation** [6520-163]
P. Yu, D. Z. Pan, The Univ. of Texas at Austin (USA)

652046  **Analysis of pattern density on process proximity compensation** [6520-165]
S. Jung, F. Lo, T.-C. Yang, T.-H. Yang, K.-C. Chen, C.-Y. Lu, Macronix International Co., Ltd. (Taiwan)

652047  **Advanced new OPC method to improve OPC accuracy for sub-90-nm technology** [6520-166]
J. Choi, J. Kang, Y. Shim, K. Yun, J. Hong, Y. Lee, K. Kim, Dongbu Electronics Co., Ltd. (South Korea)

652048  **Improving the model robustness for OPC by extracting relevant test patterns for calibration** [6520-168]
M.-G. Jeong, S.-H. Lee, J.-E. Jung, C. Hyon, I. Choi, Y.-S. Kang, Y. Park, Samsung Electronics Co., Ltd. (South Korea)

65204A  **Rapid search of the optimum placement of assist feature to improve the aerial image gradient in iso-line structure** [6520-170]
J. Li, Q. Yan, L. S. Melvin III, Synopsys, Inc. (USA)

65204C  **A feasible model-based OPC algorithm using Jacobian matrix of intensity distribution functions** [6520-172]
Y. Chen, Zhejiang Univ. (China); K. Wu, Anchor Semiconductor, Inc. (USA); Z. Shi, X. Yan, Zhejiang Univ. (China)

65204D  **Geometrical description of the microloading effect in silicon trench structures** [6520-173]
I. Titarenko, E. Altshuler, R. Tweg, Tower Semiconductors, Ltd. (Israel)

65204E  **Investigation of DFM-lite ORC approach during OPC simulation** [6520-174]
C. T. Lim, K. Peter, Y. Temchenko, D. Wallis, D. Kaiser, I. Meusel, S. Schmidt, Infineon Technologies Dresden GmbH and Co. OHG (Germany); M. Niehoff, Mentor Graphics Corp. (Germany)

65204F  **Comparing traditional OPC to field-based OPC for 45-nm node production** [6520-175]

65204S  **CDU minimization at the 45-nm node and beyond: optical, resist, and process contributions to CD control** [6520-177]
S. Scheer, M. Carcasi, Tokyo Electron America, Inc. (USA); T. Shibata, T. Otsuka, Tokyo Electron Kyushu Ltd. (Japan)

65204I  **ACLV performance dry vs. immersion on 45-nm ground rules** [6520-179]
U. P. Schroeder, Infineon Technologies NA (USA); C.-C. Yap, Chartered Semiconductors (USA); C. S. Sarma, Infineon Technologies NA (USA); A. Thomas, IBM Microelectronics (USA)
Feasibility study of 45nm metal patterning with 0.93 NA [6520-181] Y. F. Cheng, Y. L. Chou, Y. C. Hou, B. J. Lu, C. H. Yang, United Microelectronics Corp. (Taiwan)


Challenges and solutions for transferring a 248-nm process to 365-nm imaging [6520-183] A. Serebriakov, ASML Netherlands B.V. (Netherlands); C. Chang, SMIC (China); A. Becht, R. Pluijms, A. Cheng, E. Shi, H. van den Broek, L. Zhao, ASML Netherlands B.V. (Netherlands)

New color alignment for CMOS image sensor [6520-184] M. K. Dagan, Tower Semiconductor, Ltd. (Israel); R. Edart, ASML Netherlands B.V. (Netherlands); H. Rechtman, Tower Semiconductor Ltd. (Israel); Y. Kanfi, P. Warnaar, ASML Netherlands B.V. (Netherlands); O. Moshe, Tower Semiconductor, Ltd. (Israel); R. van Haren, ASML Netherlands B.V. (Netherlands)

A thin FinFET Si-fin body structure fabricated with 193-nm scanner photolithography and composite hard mask etching technique upon bulk-Si substrate [6520-185] W.-S. Liao, Y.-H. Liu, United Microelectronics Corp. (Taiwan); W.-T. Chang, United Microelectronics Corp. (Taiwan) and National Chia Tung Univ. (Taiwan); T.-H. Chen, T. Shih, H.-C. Tsen, L. Chung, United Microelectronics Corp. (Taiwan)

ARC stack development for hyper-NA imaging [6520-186] V. Farys, STMicroelectronics (France); S. Warrick, Freescale Semiconductor (France); C. Chaton, CEA-LETI (France); J.-D. Chapon, STMicroelectronics (France)

A thick CESL stressed ultra-small (Lg=40-nm) SiGe-channel MOSFET fabricated with 193-nm scanner lithography and TEOS hard mask etching [6520-187] W.-S. Liao, T.-H. Chen, H.-H. Lin, United Microelectronics Corp. (Taiwan); W.-T. Chang, United Microelectronics Corp. (Taiwan) and National Chia Tung Univ. (Taiwan); T. Shih, H.-C. Tsen, L. Chung, United Microelectronics Corp. (Taiwan)

Three-dimensional mask effects and source polarization impact on OPC model accuracy and process window [6520-188] M. Saied, Freescale Semiconductor (France); F. Foussadier, STMicroelectronics (France); J. Belledent, NXP Semiconductors (France); Y. Trouiller, CEA-LETI (France); I. Schanen, IMEP (France); C. Gardin, Freescale Semiconductor (France); J. C. Urbani, STMicroelectronics (France); P. K. Montgomery, Freescale Semiconductor (France); F. Sundermann, F. Robert, STMicroelectronics (France); C. Couderc, NXP Semiconductors (France); F. Vautrin, G. Kerrien, J. Planchot, STMicroelectronics (France); E. Yesilada, Freescale Semiconductor (France); C. Martinelli, STMicroelectronics (France); B. Wilkinson, Freescale Semiconductor (France); A. Borjon, L. Le-Cam, NXP Semiconductors (France); J. L. Di-Maria, CEA-LETI (France); Y. Rodi, NXP Semiconductors (France); N. Morgana, Photronics, Inc. (USA); V. Farys, STMicroelectronics (France)

Analysis of diffraction orders including mask topography effects for OPC optimization
[6520-190]

**POSTER SESSION: POLARIZATION, HYPER-NA, AND IMMERSION LITHOGRAPHY**

Immersion lithography with numerical apertures above 2.0 using high index optical materials [6520-191]
J. Zhou, N. V. Lafferty, B. W. Smith, Rochester Institute of Technology (USA); J. H. Burnett, NIST (USA)

Immersion defect reduction: I. Analysis of water leaks in an immersion scanner [6520-193]

Defect testing using an immersion exposure system to apply immediate pre-exposure and post-exposure water soaks [6520-194]
R. D. Watso, T. Laursen, B. Pierson, K. D. Cummings, ASML (USA)

Polarization properties of state-of-art lithography optics represented by first canonical coordinate of Lie group [6520-195]
T. Fujii, Y. Kudo, Y. Ohmura, K. Suzuki, J. Kogo, Y. Mizuno, N. Kita, Nikon Corp. (Japan); M. Sawada, Nikon System (Japan)

Characteristics analysis of polarization module on optical proximity effect [6520-196]
C. Park, J. Hong, K. Yang, Hynix Semiconductor, Inc. (South Korea); T. Theeuwes, F. Gautier, ASML (Netherlands); Y.-H. Min, A. Chen, ASML TDC Asia (Taiwan); H. Yang, D. Yim, J. Kim, Hynix Semiconductor, Inc. (South Korea)

Author Index
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Session Chairs

1 Past, Present, and Future Directions
Donis G. Flagello, ASML US, Inc. (USA)
Harry J. Levinson, Advanced Micro Devices, Inc. (USA)
2 Immersion Status and Performance
Willard E. Conley, Freescale Semiconductor, Inc. (France)
Andrew Grenville, SEMATECH, Inc. (USA) and Intel Corporation (USA)

3 Hyper-NA and Polarization
Gary Zhang, Texas Instruments Inc. (USA)
Roger H. French, DuPont Company (USA)

4 Double Patterning Technology
Robert J. Socha, ASML MaskTools Inc. (USA)
Bruce W. Smith, Rochester Institute of Technology (USA)

5 Optimization, Control, and Performance
Tatsuhiko Higashiki, Toshiba Corporation (Japan)
Wilhelm Maurer, Infineon Technologies AG (Germany)

6 OPC and Advanced Modeling I
Eric Hendrickx, IMEC (Belgium)
Kafai Lai, IBM Corporation (USA)

7 Image Quality and Characterization
Koichi Matsumoto, Nikon Corporation (Japan)
John Lin, Taiwan Semiconductor Manufacturing Company, Ltd. (Taiwan)

8 Challenges for Water Immersion
Akiyoshi Suzuki, Canon Inc. (Japan)
Pary Baluswamy, Micron Technology, Inc. (USA)

9 Computational Lithography: Joint Session with Conference 6521
Alfred K. K. Wong, Magma Design Automation (USA)
Donis G. Flagello, ASML US, Inc. (USA)

10 Advanced Resolution Enhancement
Harry J. Levinson, Advanced Micro Devices, Inc. (USA)
Tatsuhiko Higashiki, Toshiba Corporation (Japan)

11 Mask Effect and Technologies
Wilhelm Maurer, Infineon Technologies AG (Germany)
Pary Baluswamy, Micron Technology, Inc. (USA)

12 Immersion Advancements beyond Water
Andrew Grenville, SEMATECH, Inc. (USA) and Intel Corporation (USA)
Bruce W. Smith, Rochester Institute of Technology (USA)

13 OPC and Advanced Modeling II
Bruce W. Smith, Rochester Institute of Technology (USA)
Donis G. Flagello, ASML US, Inc. (USA)
14 Advanced Exposure Systems and Components I
Akiyoshi Suzuki, Canon Inc. (Japan)
Gary Zhang, Texas Instruments Inc. (USA)

15 Advanced Exposure Systems and Components II
Kurt G. Ronse, IMEC (Belgium)
Koichi Matsumoto, Nikon Corporation (Japan)
Lithography Beyond 32nm – A Role for Imprint?

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Abstract

Imprint lithography has been used since the application of the Chinese wax seal to authenticate official documents. In the past century the resolution of the technology has been driven through commercial applications such as vinyl records, CDs and more recently by high definition DVDs. In the past decade, high resolution imprinting has extended the resolution down to sub 10nm features and this fact, coupled with the low cost of the tool, make it attractive as an alternative to other lithographic technologies.

More recently the evolution of imprint lithography from thermal imprinting to UV cured materials, has allowed the technology to operate at room temperature (allowing tight overlay) and low material viscosities (important for high throughput), opening up the potential for CMOS applications. This paper will discuss recent progress in align/overlay, throughput, defect density, materials and the availability of sub 20nm templates, along with tool developments, that make the technology a viable option for advanced CMOS beyond 32nm HP design nodes.

In addition, imprint lithography is being developed for other large electronic markets such as bit patterned media (BPM) for disk drives, and photonic crystals to increase the brightness and efficiency of LEDs used for solid sate lighting, both of which applications are likely to go into production ahead of sub 32nm CMOS. Since overlay requirements are significantly less, whole wafer (as opposed to step and repeat) imprinting is used for these applications, and the presentation will discuss the synergies with CMOS imprint technology.

Key words: Imprints lithography, photolithography, bit patterned media, photonic crystals,

1. Introduction

Despite the remarkable progress made in the past decade in extending optical lithography to deep sub-wavelength imaging, the limit for the technology seems to be fast approaching. At 22nm half pitch design rules, neither very high NA tools (NA 1.6), nor techniques such as double patterning, are likely to be sufficient. The extension of photon based systems to EUV remains very challenging, and this has opened up the opportunity for imprint lithography as a very viable NGL alternative.

Small feature imprint lithography has existed for several years.(1-7) The original technique involved the use of a patterned template which is impressed onto a thermo plastic material and, with the combination of heat and pressure, the pattern in the template was transferred to the substrate.(2) Compact disks were one of the early applications for the technology. Recently the technique has been significantly improved with the development of Step and Flash Imprint Lithography (S-FIL™).(1) This technique was invented by Professors Grant Willson and SV Sreenivasan at the University of Texas, and involves deposition of a low viscosity monomer on the substrate, lowering a template into the fluid which then flows into the patterns of the template. Following this fill step, the monomer is exposed to UV light to cross-link it and convert it into a solid, and the template is removed leaving the solid pattern on the substrate.(1,3) The advantages of this development (low pressure imprinting, low viscosity template filling and room temperature operation) make it uniquely capable for CMOS applications. Although this paper, and this conference, are largely focused on CMOS, it is worth noting that imprint technology can also be used in a wide variety of other advanced applications, many of which are only commercially viable given the availability of low cost (sub $2M) tools capable of delivering sub 50nm features. These applications include the use of photonic bandgap crystals to
enhance LED efficiency and brightness, patterned media for disk drives, polarizers for projection optical engines and a wide variety of other electronic and photonic devices. For most of these applications the capital cost of 193nm immersion lithography is commercially untenable, even assuming that the required resolution limits could be reached.

The purpose of this paper is to describe the recent advances in imprint lithography with particular reference to its application for silicon integrated circuits.

2. Imprint Technology for CMOS Applications

The S-FIL process is shown schematically in Figure 1. The process starts with a template made from a standard 6025 photomask blank, with the pattern etched into the glass using the same technology that is used for phase shift masks. An array of pico-liter sized drops of a low viscosity monomer, are spread across the field being imprinted and the template lowered onto the drops. When the surface tension of the liquid has been broken, capillary action draws the fluid into the template features. Once filling is complete, ultraviolet light, passing through the glass template, is used to cross link the monomer and convert it to a solid. The template can then be withdrawn and the process repeated on the next field.

The use of a low viscosity liquid has several advantages over spin-on films. Firstly, the lower viscosity of the liquid means that material movement and filling of the template are faster, particularly since the drop pattern density can be matched to the pattern density on the template. Secondly the process is intrinsically lower pressure – in fact controlled by capillary action, which also assures that the fluid does not spread outside of the template field. Finally, the use of the “drop on demand” technique prevents the requirement that spin coated wafers be passed into the tool – avoiding the problems of materials evaporation, particle collection on “wet” wafers and the need for a linked track. Since the pattern is “fixed” by UV light, the whole process can be completed at a controlled temperature allowing tight overlay between levels.

Molecular Imprints has commercialized the S-FIL technology, offering a CMOS compatible imprint tool – the Imprio-250™ - which has been designed to take advantage of this type of imprint lithography, and offers the capability of mix and match with 193nm optical lithography with a 26mmx33mm field size, alignment/overlay and magnification control, automated imprint and FOUP to FOUP wafer handling. A photograph of the Imprio-250 is shown in Figure 2.

3. The Advantages and Challenges for Imprint Lithography

Imprint lithography has a number of distinct advantages over photolithography when used for CMOS applications. These include:

(i) Lithographic capability

The imprint process appears to perfectly replicate the template. In consequence the template controls the resolution, line edge roughness and CD control of the imprinted pattern. Since the template has to be only written once, great care can be taken to assure its fidelity. Resolution limits appear to be less than 5nm. An example of research work from the University of Illinois (7) is shown in Figure 3, where a carbon nano-tube based template was replicated – if not perfectly. Since the monomer is of low molecular weight and is physically constrained by the template during solidification, there are none of the resolution/LER issues of molecular size, acid diffusion or areal image that are present in optical lithography. Other data/examples of lithographic quality are shown in Figures 10,12 & 13 and are discussed later in the text.
(ii) No OPC/RET/MEEF or design rule restrictions

Since the template is faithfully replicated by the imprint process – topics such as OPC and MEEF have no meaning in imprint lithography. While manufacturing a 1x template does present some additional challenges – it provides the device designer with complete freedom to design circuits without any lithography based design rules, freeing the designer from optical modeling artifacts. It is truly a “what you see is what you get” technology.

(iii) Lower capital cost

Since imprint tools lack the very complex lens and mirror systems inherent in photon based technologies, nor the need for a linked track, nor the requirement for vacuum and complex sources in EUV, the cost of the tools are significantly less than their competition. In addition, since they are largely mechanical tools, the build times are markedly less.

(iv) 3D printing

Since multi-level or curved features can be built into the templates, the technology has the capability for three-dimensional printing. This has the potential to extend the technology well beyond simple resist and etch capability and into the realm of single step imprinting of dual damascene structures (multilevel features) or direct imprinting of micro-lenses for CMOS imaging devices (curved features). These applications will be discussed later in the paper.

However, as might be expected, these advantages also come with a set of companion challenges. Confronting the technical challenges listed below is the topic of the main portion of this text, but they are listed below in summary form and to provide balance to the advantages.

(i) 1x templates – higher resolution, image placement and defect requirements as compared to 4x photomasks

(ii) Defect concerns – near contact printing

(iii) Throughput – in contrast to photolithography that simply requires exposure for each field, imprint requires not only exposure, but also material dispense, template fill, and field by field alignment.

(iv) Overlay – issues of mechanical magnification control

4. Technical Progress in Imprint Lithography for CMOS Applications

4.1 Templates

Imprint lithography uses templates made with commercial photomask materials and processes. This is a significant advantage relative to previous NGL technologies (X-Ray Proximity and Electron Beam Projection) that struggled with membrane based masks, or even EUV that requires new substrates and reflecting metal films. However, the 1X requirement does test resolution related issues – although not as near to the 4X that might come to mind. The advent of OPC features, which will soon be no more than 1.3x the minimum feature size on the wafer \(^8\) are accelerating the resolution of mask ebeam writers. In addition for imprint templates, since the chrome is only being used as an etch mask (no optical opacity requirements), it is possible to use thinner chrome and ebeam resist than is typical to push resolution down to the required 1x. Image placement is also an issue for a 1x technology, but again, the approaching application of double patterning for 193nm immersion is pressing the existing photomask industry to meet very tight image placement specifications, even for nominally 4x photomasks.
Using commercially available VSB mask writers, imprint templates are already being written down to 35nm dimensions, with very high quality, as shown in Figure 4a. For higher resolution applications, imprint templates can be written with variants of ebeam direct write tools, usually Gaussian Beam systems. These tools have unparalleled resolution, and can easily produce templates with dimensions of less than 20nm as shown in Figure 4b providing an imprint resolution capability well beyond that possible with existing optical technologies.

However resolution is not the only issue for ebeam pattern generators, although it is the most compelling one for device/process development engineers pushing down below 30nm. Photomask write times have been rising rapidly in the past few years – victims of the huge data files required for advanced OPC. Templates have certain advantages in this area. Firstly there are no OPC features required, significantly reducing the number of shots required, and secondly, the area to be written is also a lot smaller. In addition, it is possible to “replicate” template patterns. In this process a single die template is made using an ebeam pattern generator, and then an imprint tool, such as the Imprio-250, is used to replicate this die to create a full field template containing multiple die. For a high volume runner, with four die per field and requiring five mask sets, the effective ebeam write acceleration would be a factor of 20 (four die X five mask sets). This technique has been used in the past for whole wafer, non-CMOS, imprint applications, and an example of the efficacy of the replication process is shown in Figure 5. The potential for lowering write times for imprint templates is important since it opens up the potential to use less sensitive ebeam resists to make the templates. This in turn allows templates with superior line edge roughness and higher resolution.

Template inspection and repair is also an issue since printable features are four times smaller than those for photomasks. To date the most sensitive template inspection techniques have used 1x wafer inspection tools. The KLA ES-32 tool has proved to be effective in detecting sub 50nm defects using a die to die approach as shown in Figure 6a. For die to data base results, NGR has been able to detect 20nm defects using its 2100 tool, as shown in Figure 6b. Repair of template defects can either be completed by mechanical removal of excess material using a Rave 650NM tool, or by replacing missing material using a Nowatech MeRiTM ebeam enhanced deposition system. Examples of repair are shown in Figure 7. In the case of imprinting, the repairs are required to fill or remove material to a particular thickness, in contrast to a particular optical opacity. Small variations away from the nominal required dimensions are acceptable since this would simply mean that the imprinted resist thickness was slightly different from nominal.

4.2 Alignment and Overlay

All imprint tools for CMOS applications must be designed to mix and match with existing 193nm optical lithography tools. This requires a step and repeat tool with a 26mmx33mm field size, alignment marks that fit into 75µm streets, alignment systems with sufficient contrast and show overlay results on top of 193nm printed under-layers.

The Imprio-250 uses a field by field alignment system, originally conceived for use in X-ray proximity printing, an earlier NGL technology. This does not add to the imprint time since the alignment occurs during the time that the fluid is filling the template features. The “in liquid” align has the advantage that the imprint fluid acts both as a vibration damper and also a lubricant to facilitate the small motions required between the template and the substrate during alignment, reducing stiction effects.

Since the template and substrate are in close proximity (<10µm) during the alignment process, it is practical to capture the relative positioning error between two matching alignment marks using a Moiré image based technique. The advantage of using a 1st order Moiré image based technique is that it can provide high resolution alignment data using a low NA imaging unit (<0.05) without blocking the UV beam path. The alignment system utilizes multiple imaging units that can capture not only x, y, theta but also magnification errors. Utilizing the gap insensitiveness of the 1st order Moiré alignment data can be captured throughout the template fill step and corresponding correction motions are accomplished in a
parallel manner. This system has demonstrated better than 1nm sensitivity of the alignment and positioning system. (16, 18)

Magnification correction is achieved by mechanically compressing the template. Positive magnification can be achieved by writing the template 5ppm oversize and releasing the compression. In this way the required +/- 5ppm can be obtained. Since the distortion is this small, well within the elastic regime of the material, it is perfectly reversible. A multi-point forcing mechanism was developed\(^1\) that can induce optimized vectors of correction forces along the periphery of the template. Such an optimized forcing vector for the mag/distortion correction is computed using multiple relative position data between the template and the wafer that are captured using the alignment system described above. When n-points of forcing per template side are utilized, a vector with a 4n-3 controllability, where 3 stands for three constraints, is available. Therefore, a typical alignment for x, y, theta, mag x, mag y and orthogonality can be compensated.

The efficacy of the alignment and magnification control systems were tested using a KLA overlay tool and AIM/Archer alignment marks. A sample set of results\(^2\) are shown in Figure 8 with approximately 20nm 3 sigma overlay measured for 32 fields and 81 points per field. The major sources of the error are thought to be from thermal distortions, placement errors on the template and image field distortions from the 193nm scanner. Further improvements are expected to reduce the overlay errors down to 5nm.

4.3 Throughput

While slower throughputs may be acceptable for early unit process development and device prototyping, it is clear that production needs of 20wph are required almost regardless of cost of ownership. This represents a challenge for imprint, since it is a multi-step process (fill, overlay, cure etc). The required budget to imprint a field at 20 wph is shown in Table 1.

<table>
<thead>
<tr>
<th>Stage move, fluid dispense time</th>
<th>0.15 seconds</th>
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<tbody>
<tr>
<td>Alignment, template fill time</td>
<td>1.00 seconds</td>
</tr>
<tr>
<td>UV cure time</td>
<td>0.15 seconds</td>
</tr>
<tr>
<td>Separation time</td>
<td>0.10 seconds</td>
</tr>
<tr>
<td>TOTAL</td>
<td>1.40 seconds</td>
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The most significant budget item, and the one specific to imprint, is the time required to fill the template. The two key parameters for fast fill are firstly, drop size and placement and secondly, the template contact angle to minimize any trapped air bubbles. In this latter respect, care must be taken to lower the template in a controlled and inclined angle such that the drops coalesce in a wave front that allows the gas between the drops to be swept out rather than trapped between the drops. The size and placement of the drops are carefully controlled to facilitate this. To do this, the drops, with a size of a few pico-liters, are dispensed using a linear array of several hundred inkjet nozzles that sweeps across the 26x33mm field. The density and pattern of the drops are automatically slaved to the GDS-II file used to create the template, such that the density of the drops is optimized to the template pattern to minimize the amount of material movement required to fill the template features. Under optimal conditions fill times as low as 3 seconds have been achieved in the laboratory and further improvements are expected. The viscosity of the imprint fluid is also an issue relative to fill times. Acrylate based materials (see Section 5.1 below) have viscosities in the 5-10cps range, and other materials such as vinyl ethers are closer to 1 cps.

Future tool designs could use two other advantages inherent to imprint to improve the throughput. The ability to imprint larger field sizes could allow future systems to print four 26mmx33mm fields at once. This would place significant additional requirements on the template fabrication and overlay, but quadruple the throughput. In addition, since the cost of the imprint heads is minimal relative to optical lens stacks, multiple heads could be placed on a single stage platform, further increasing throughput, although multiple templates would be needed.
4.4 Defects

There is concern about the defect levels inherent in imprint lithography since it is a near contact technology. However, it is an error to assume that the problem is similar to that of contact printing for the following reasons:

(i) The template never actually touches the substrate. There is always a thin residual film of imprint material between the two surfaces.
(ii) The imprint fluid drops, which have micron height, tend to cushion any impact between the template and particles.
(iii) The template is made from fused silica – a hard and robust material.

Significant progress has been made in reducing the defectivity of CMOS imprints. This progress is shown in Figure 9. While still a considerable distance from what is ultimately needed for CMOS production, the progress has been sufficient for early device development activities. A Pareto analysis shows the defects to have three major sources: template defects, imprint specific defects and particles.

Template defects, as supplied by the commercial photomask vendors are, as might be expected, typically less than 1cm⁻² as measured on a KLA 576 inspection tool. The template defect level is increased somewhat by the post photomask processing specifically required for templates (dice and polish, mesa preparation) but this does not represent an insuperable problem. The major challenge is to extend the life of the templates prior to their need to be removed from the imprint tool and re-cleaned. The templates do not “wear-out” since the fused silica is not eroded in anyway by contact with the imprint fluid. However, they can, over time, pick-up defects from partially cured monomer, or other contaminants, after several thousand imprints and need to be cleaned. Since the monomer is organic, the cleaning process is a standard oxidative clean, and early results for in-situ gas phase cleaning show some promise.

Imprint specific defects (micro-bubbles, imprint feature pull-outs etc) have been reduced to ~1cm⁻². One important piece of data further suggests that these defects are not very dependent on defect size. A sample of imprinted patterns was tested on a KLA 2132 optical inspection tool with a 200nm pixel size and then retested on a KLA ES32 electron beam tool with a 25nm pixel size. The comparison of the results is shown in Table 2.

Table 2 – 200nm and 25nm Pixel Inspection Results

<table>
<thead>
<tr>
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<th>KLA 2132 (200nm)</th>
<th>KLA ES32 (25nm)</th>
</tr>
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<tbody>
<tr>
<td>Template defects</td>
<td>4.8cm⁻²</td>
<td>6.0cm⁻²</td>
</tr>
<tr>
<td>Particles</td>
<td>2.4cm⁻²</td>
<td>19.7cm⁻²</td>
</tr>
<tr>
<td>Imprint specific defects</td>
<td>0.0cm⁻²</td>
<td>0.0cm⁻²</td>
</tr>
</tbody>
</table>

Although this was an experiment with relatively low inspected area, the lack of defect size dependence for both the template defects and the imprint specific defects is very important since it suggests that the density of these defects is not strongly correlated with size. This is not altogether surprising when considered more deeply. For example micro-bubbles are know to be less stable the smaller they become, and imprint feature pull outs are more dependent on aspect ratio than feature size. The increase in particles as the resolution of the defect detection improved was to be expected. Further work in a cleaner environment, will reduce these numbers.

5. Materials and Processes

For imprint lithography to be successful in CMOS, a complete solution must be available including materials and processes to complement the tool and templates.
5.1 Materials

Successful imprint materials must be formulated with consideration for many requirements and the resulting formulations tend to be very sophisticated \(^{(22)}\) to meet the severe yield demands for CMOS. The majority of the work described below is built around an acrylate backbone, but vinyl ethers \(^{(23)}\) have also been used.

One of the most basic challenges for imprint lithography is how to assure that the material sticks to the substrate and not to the template, even after many thousands of imprints. To reduce the surface energy of the template, a high surface concentration of fluorine is required, but this then restricts the wettability and filling speed, requiring a delicate balance. In addition, any coating on the template is liable to wear and tear, and an in-situ replenishment/repair process is required to keep the defectivity levels down. On the wafer surface, an adhesion promotion film can be used, but needs to be very thin (<2nm) and must be formulated to assure adhesion to multiple surface materials and also with a mind to wettability.

The cross linked material has to be drawn out of the template features during separation. This mandates a material with adequate mechanical strength, toughness and Young’s Modulus to maximize the aspect ratio that can be used and yet completely prevent the possibility of a feature being left in the template. Adding polar components helps with these properties but excessive amounts increases the surface tension and reduces the fill speed. The etch resistance must be equivalent to the photoresists. The material must be formulated to be sensitive to UV radiation to assure fast curing, which means attention must be paid to the photoinitiators, the wavelength of the exposing light and the prevention of oxygen inhibition.

Viscosity must be controlled. Low viscosities (<5cps) assist faster feature filling, \(^{(24)}\) but higher viscosities (10-20cps) tend to be more favorable for ink-jet dispense into pico-liter drops. Lower viscosity materials tend to have high vapor pressures and evaporation rates which need to be minimized or compensated for.

Finally the purity of the material must meet the stringent CMOS requirements of <10ppb (metal ions), not just as formulated, but after passage through the inkjet head assembly.

5.2 Process

For imprint to be successful for CMOS, the tools must not only mix and match with 193nm optical tools, but the imprint materials and processes have to be compatible with the upstream and downstream CMOS processing as well. Most CMOS customers want to place the imprint process into their integrated process without any changes – essentially a drop in replacement for optical lithography.

This has been achieved with the use of the SFIL-O process shown in Figure 1. In this process the organic imprint material has been formulated to be an effective etch mask for silicon based films, and the imprint process tuned to the point where the residual organic layer between the imprinted features is both very thin (~15nm) and very uniform (<5nm 3σ). Since the imprinted features have a typical height of over 50nm (2.5:1 aspect ratio for 22nm HP features), the residual layer can be removed with a quick “de-scum” oxygen etch, prior to etching the hard mask with a fluorine based etch. Typical results for hard mask etching are shown in Figure 10.\(^{(25)}\) Excellent resolution, line edge roughness and sidewall angle are routinely achieved. Typical etch ratios between the imprinted material and the underlying hard mask are designed to mimic 193nm photoresists, so that the etching processes can be very similar.

An alternative process called SFIL-R \(^{(26)}\) has been developed to provide a positive image of the template on the substrate (as opposed to the negative working SFIL-O process). In this case, following imprinting, a silicon containing film is spun on top of the imprinted features, effectively planarizing the surface. A blanket etch back of the silicon film is made until the imprinted organic features are exposed. At this point the etch chemistry is changed to an oxidative etch which then removes the underlying imprinted features, but leaves the silicon containing material between them intact to act as an etch mask. The SFIL-R process has the advantage of being less sensitive to surface topography on the substrate.
Imprinting has a unique advantage over photolithography, in that one can make multilevel template features. There has been growing interest in the use of multi-level template imprinting to define both levels of a dual damascene pattern with a single step.\(^{(27)}\) This can be done in one of two ways. In the first case, a deposited low-k film is patterned with a double level template to pattern both the via and channel features with an imprinted resist. This resist pattern is then etched down to replicate the pattern in the low-k material. This requires that the resist and low-k film etch at the same rate, but surprisingly good results have been achieved.\(^{(28)}\) Given the large number of metal levels on advanced logic devices, this offers the potential for significant reduction in cost, and at feature sizes that may be more compatible with 1x template technology. An even greater cost reduction can be achieved, if the low-k material is directly imprinted in one step. This presents many challenges for the material – which must now not only be a viable imprint material but also a viable low-k material as well. However, significant progress has been made in this area, both in terms of material\(^{(29,30)}\) and process\(^{(29)}\) as shown in Figure 11.

6. Application of Imprint to CMOS

As mentioned at the start of this paper, the most likely production entry point for imprint in CMOS will be at or below the 32nm half pitch node. While the production ramp date for these technology nodes will be out into the next decade, R&D engineers are beginning to require sub 32nm lithography for unit process development (UPD) and device prototyping. This is an excellent application for imprint lithography since sub 32nm resolution is easily obtained, the SFIL-O process is fully compatible with existing hard mask etch processes, and the absence of liquid development means that pattern collapse is not an issue. Examples of CMOS UPD patterns are shown in Figure 10.\(^{(25)}\)

Further extensions to device prototyping require capability for overlay in addition to resolution. For example, IBM recently announced results\(^{(31)}\) on device designs that require densities down to 10nm HP for economic feasibility. Progress with imprint lithography has allowed device structures to begin approaching these dimensions as shown in Figure 12.\(^{(32)}\) The 27nm silicon fin structures, built on an SOI substrate, were patterned using SFIL-O imprint lithography, followed by plasma etching with a SiN hardmask. The etched cross sections illustrated in Figure 12, show excellent line edge roughness, CD control and sidewall angles for the etched silicon fins.

Unlike other CMOS NGL technologies, imprint lithography is also applicable to other markets which have similar resolution demands as CMOS, but are likely to go into volume production at an earlier date. One example\(^{(33)}\) is bit patterned media (BPM) for hard disk drives. This technology, expected to ramp at the end of this decade, is required since magnetic confinement of the domain is inadequate below 20nm (>500Gb/sq inch density), and beyond this requires the magnetic domains to be individually etched into the magnetic film on the disk. An example is shown in Figure 13.\(^{(34)}\) Imprint is the preferred solution for this application given the lower cost and ability to print larger fields (up to 3.5” disks) when compared to photolithography. With over a billion disk drives produced each year, this market alone will be hundreds of tools. The early application to BPM at 20nm will help develop the commercial infrastructure for templates, materials and process technology.

A second non-CMOS market is patterning high brightness LEDs with photonic crystals. These structures look like arrays of contact holes on the surface of the LED and serve to increase both the brightness and the efficiency of the LED.\(^{(35)}\) The feature sizes need to be less than the wavelength of the LED emission, and the minimum hole spacing can be significantly less than 100nm. Given the poor surface flatness, and 3” dimensions, of the GaN substrates used for these devices, optical lithography is difficult to use for these dimensions, and imprint lithography is the preferred solution. Photonic crystal enhanced LEDs are beginning to appear in commercial\(^{(36)}\) quantities and with broad markets such as back lit flat panel displays, architectural lighting and automotive headlights, this application will also require large numbers of imprint tools over the next five years.

Both the BPM and LED can tolerate lower overlay than CMOS (1-3µm) and the lowest cost of ownership comes from printing the whole substrate at once. Molecular Imprints has developed a companion tool\(^{(37)}\) to the I-250, the I-1100 shown in Figure 14, to handle whole wafer imprinting. Like the I-250, the I-1100 is a
fully automated, cassette to cassette manufacturing tool, but uses a thinner, compliant template to allow for the greater non-flatness of the non-silicon wafers.

7. Summary

Imprint lithography has made remarkable improvements over the past five years. The advent of drop on demand, step and flash technology has resulted in significant improvements in overlay, defect density and throughput, such that this technology is now a very viable contender for CMOS NGL. Concurrent improvements in template fabrication, materials and process mean that the technology can be used as a drop in replacement for photolithography but at much higher resolutions and lower cost than competing technologies such as EUV.

8. Acknowledgements

The authors would like to thank the many members of Molecular Imprints and other companies who provided data for this paper. This work was partially funded by DARPA Contract No. N66001-02-C-8011, NIST Advanced Technology Program Contract No. 70NANB4H3012, and DoD Contract No. N66001-06-C-2003.

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Figures

**Figure 1.** Schematic of the SFIL-O process

Step 1: Dispense Drops

Step 2: Lower Template and Fill Pattern

Step 3: UV Polymerizes Imprint Fluid

Step 4: Separate Template from Substrate

**Figure 2.** Imprio-250 tool for CMOS

**Figure 3.** UV cured imprints showing sub 5nm resolution. Top micrograph is the template, lower micrograph the imprinted image. From ref 7.

**Figure 4a.**

**Figure 4 b.**

**Figure 4.** Showing 1x template patterns. Top micrograph from VSB pattern generators. Lower micrographs from Gaussian Beam tools. From ref 9 and 11.
Figure 5: Template replication results. Left hand micrograph shows imprinted features from the ebeam master template, the right hand micrograph shows imprinted features from the replicated template.

Figure 6a

Figure 6b

Figure 6: Template defect inspection results. Fig 6a showing ES-32 inspection down to sub 30nm resolution (from ref 12) and Fig 6b showing die to data base results at 20nm (from ref 13).

Figure 7a

Figure 7b

Figure 7: Template defect repair results. Fig 7a showing mechanical removal of defect (from ref 14) and Fig 7b showing repair of a missing defect using ebeam enhanced deposition (from ref 15).
Figure 8: Overlay data from imprint patterns over 193nm optically exposed underlayers. 32 fields per wafer and 81 locations per field (from ref 20)

Figure 9: Defect improvement over time for SFIL. (from ref 21)
Figure 10: Cross section and top view images of 32nm half pitch imprinted features showing excellent wall angle and line edge roughness (from ref 25, with a template made by DNP).

Figure 11: Imprinted low-k dual damascene results showing the top view of the imprinted low-k dielectric and a cross section after barrier metal and copper fill (from ref 29).

Figure 12: Cross section views of experimental device from IBM (ref 32). Top micrograph, 27nm silicon fins, imprinted and etched; lower micrograph, cross section of the device.

Figure 13: Sub 30nm half pitch patterns for BPM (from ref 34).

Figure 14: Imprio-1100Whole wafer, conformal imprinter for LED, optical component and BPM applications.