PROCEEDINGS OF SPIE

SPIDigitalLibrary.org/conference-proceedings-of-spie

Front Matter: Volume 7973

, "Front Matter: Volume 7973," Proc. SPIE 7973, Optical Microlithography XXIV, 797301 (5 May 2011); doi: 10.1117/12.894750

SPIE.

Event: SPIE Advanced Lithography, 2011, San Jose, California, United States

PROCEEDINGS OF SPIE

Optical Microlithography XXIV

Mircea V. Dusa

Editor

1–3 March 2011

San Jose, California, United States

Sponsored

SPIE

Cosponsored by

CYMER Inc. (United States)

Published by

SPIE

Volume 7973

Proceedings of SPIE, 0277-786X, v. 7973

SPIE is an international society advancing an interdisciplinary approach to the science and application of light.

The papers included in this volume were part of the technical conference cited on the cover and title page. Papers were selected and subject to review by the editors and conference program committee. Some conference presentations may not be available for publication. The papers published in these proceedings reflect the work and thoughts of the authors and are published herein as submitted. The publisher is not responsible for the validity of the information or for any outcomes resulting from reliance thereon.

Please use the following format to cite material from this book:

Author(s), "Title of Paper," in *Optical Microlithography XXIV*, edited by Mircea V. Dusa, Proceedings of SPIE Vol. 7973 (SPIE, Bellingham, WA, 2011) Article CID Number.

ISSN 0277-786X

ISBN 9780819485328

Published by

SPIE

P.O. Box 10, Bellingham, Washington 98227-0010 USA

Telephone +1 360 676 3290 (Pacific Time) · Fax +1 360 647 1445

SPIE.org

Copyright © 2011, Society of Photo-Optical Instrumentation Engineers

Copying of material in this book for internal or personal use, or for the internal or personal use of specific clients, beyond the fair use provisions granted by the U.S. Copyright Law is authorized by SPIE subject to payment of copying fees. The Transactional Reporting Service base fee for this volume is \$18.00 per article (or portion thereof), which should be paid directly to the Copyright Clearance Center (CCC), 222 Rosewood Drive, Danvers, MA 01923. Payment may also be made electronically through CCC Online at copyright.com. Other copying for republication, resale, advertising or promotion, or any form of systematic or multiple reproduction of any material in this book is prohibited except with permission in writing from the publisher. The CCC fee code is 0277-786X/11/\$18.00.

Printed in the United States of America.

Publication of record for individual papers is online in the SPIE Digital Library.

SPIDigitalLibrary.org

Paper Numbering: Proceedings of SPIE follow an e-First publication model, with papers published first online and then in print and on CD-ROM. Papers are published as they are submitted and meet publication criteria. A unique, consistent, permanent citation identifier (CID) number is assigned to each article at the time of the first publication. Utilization of CIDs allows articles to be fully citable as soon they are published online, and connects the same identifier to all online, print, and electronic versions of the publication. SPIE uses a six-digit CID article numbering system in which:

- The first four digits correspond to the SPIE volume number.
- The last two digits indicate publication order within the volume using a Base 36 numbering system employing both numerals and letters. These two-number sets start with 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B ... 0Z, followed by 10-1Z, 20-2Z, etc.

The CID number appears on each page of the manuscript. The complete citation is used on the first page, and an abbreviated version on subsequent pages. Numbers in the index correspond to the last two digits of the six-digit CID number.

Contents

Part One

xv *Conference Committee*

FREEFORM AND SMO

- 7973 05 **Freeform and SMO (Invited Paper)** [7973-04]
R. Socha, ASML (United States)
- 7973 06 **Qualification, monitoring, and integration into a production environment of the world's first fully programmable illuminator** [7973-05]
G. McIntyre, IBM Advanced Lithography Research (United States); D. Corliss, IBM Microelectronics (United States); R. Groenendijk, R. Carpaij, T. van Niftrik, ASML (Netherlands); G. Landie, STMicroelectronics (United States); T. Tamura, Renesas (Japan); T. Pepin, J. Waddell, J. Woods, ASML (Netherlands); C. Robinson, K. Tian, IBM Microelectronics (United States); R. Johnson, S. Halle, IBM Advanced Lithography Research (United States); R.-H. Kim, GLOBALFOUNDRIES Inc. (United States); E. Mclellan, IBM Advanced Lithography Research (United States); H. Kato, Toshiba Corp. (United States); A. Scaduto, C. Maier, M. Colburn, IBM Advanced Lithography Research (United States)
- 7973 08 **Design specific joint optimization of masks and sources on a very large scale** [7973-07]
K. Lai, M. Gabrani, D. Demaris, N. Casati, IBM Corp. (United States); A. Torres, Mentor Graphics Corp. (United States); S. Sarkar, P. Strenski, S. Bagheri, IBM Corp. (United States); D. Scarpazza, A. E. Rosenbluth, D. O. Melville, A. Wächter, J. Lee, V. Austel, M. Szeto-Millstone, K. Tian, F. Barahona, T. Inoue, M. Sakamoto, IBM Corp. (United States)

SOURCE AND MASK OPTIMIZATION I

- 7973 09 **Illuminator predictor for effective SMO solutions** [7973-08]
D. G. Smith, Nikon Research Corp. of America (United States); N. Kita, N. Kanayamaya, R. Matsui, Nikon Corp. (Japan); S. R. Palmer, Nikon Research Corp. of America (United States); T. Matsuyama, Nikon Corp. (Japan); D. G. Flagello, Nikon Research Corp. of America (United States)
- 7973 0A **Full-chip source and mask optimization** [7973-09]
M.-C. Tsai, S. Hsu, L. Chen, Y.-W. Lu, J. Li, F. Chen, H. Chen, J. Tao, B.-D. Chen, H. Feng, W. Wong, W. Yuan, X. Li, Z. Li, L. Li, R. Dover, H. Liu, J. Koonmen, ASML Brion Technologies (United States)
- 7973 0B **Joint optimization of layout and litho for SRAM and logic towards the 20nm node using 193i** [7973-10]
P. De Bisschop, B. Laenens, IMEC (Belgium); K. Iwase, Sony Corp. (Belgium); T. Yao, Fujitsu Semiconductor Europe (Belgium); M. Dusa, ASML (Belgium); M. C. Smayling, Tela Innovations, Inc. (United States)

- 7973 0C **Applicability of global source mask optimization to 22/20nm node and beyond** [7973-11]
K. Tian, IBM Corp. (United States); M. Fakyry, A. Dave, A. Trichtkov, Mentor Graphics Corp. (United States); J. Tirapu-Azpiroz, IBM Corp. (United States); A. E. Rosenbluth, D. Melville, IBM Thomas J. Watson Research Ctr. (United States); M. Sakamoto, T. Inoue, IBM Research, Tokyo (Japan); S. Mansfield, A. Wei, Y. Kim, IBM Thomas J. Watson Research Ctr. (United States); B. Durgan, K. Adam, G. Berger, G. Bhatara, Mentor Graphics Corp. (United States); J. Meiring, IBM Corp. (United States); H. Haffner, Infineon Technologies North America Corp. (United States); B.-S. Kim, SAMSUNG Electronics Co., Ltd. (United States)
- 7973 0D **Supreme lithographic performance by simple mask layout based on lithography and layout co-optimization** [7973-12]
K. Tsujita, T. Arai, H. Ishii, Y. Gyoda, K. Takahashi, Canon Inc. (Japan); V. Axelrad, Sequoia Design Systems, Inc. (United States); M. C. Smayling, Tela Innovations, Inc. (United States)

DOUBLE PATTERNING I

- 7973 0E **Simultaneous OPC and decomposition for double exposure lithography** [7973-13]
S. Banerjee, K. B. Agarwal, IBM Research (United States); M. Orshansky, The Univ. of Texas at Austin (United States)
- 7973 0F **Towards manufacturing of advanced logic devices by double-patterning** [7973-14]
C. Koay, S. Halle, S. Holmes, K. Petrillo, M. Colburn, IBM Corp. (United States); Y. van Dommelen, A. Jiang, M. Crouse, ASML (United States); S. Dunn, Tokyo Electron America, Inc. (United States); D. Hetzer, S. Kawakami, Tokyo Electron Technology Ctr., America, LLC (United States); J. Cantone, Tokyo Electron America, Inc. (United States); L. Huli, M. Rodgers, B. Martinick, Univ. at Albany (United States)
- 7973 0G **Innovative self-aligned triple patterning for 1x half pitch using single "spacer deposition-spacer etch" step** [7973-15]
B. Mebarki, H. D. Chen, Y. Chen, A. Wang, J. Liang, K. Sapre, T. Mandrekar, X. Chen, P. Xu, P. Blanko, C. Ngai, C. Bencher, M. Naik, Applied Materials (United States)
- 7973 0H **DPT restricted design rules for advanced logic applications** [7973-16]
Y. Deng, Y. Ma, H. Yoshida, J. Kye, H. J. Levinson, GLOBALFOUNDRIES Inc. (United States); J. Sweis, T. H. Coskun, V. Kamat, Cadence Design Systems, Inc (United States)
- 7973 0I **Scanner alignment performance for double patterning** [7973-17]
L. Lattard, CEA-LETI (France); M. McCallum, R. Morton, Nikon Precision Europe GmbH (Germany); C. Lapeyre, CEA-LETI (France); K. Makino, A. Tokui, N. Takahashi, T. Fujiwara, Nikon Corp. (Japan)
- 7973 0J **Effective decomposition algorithm for self-aligned double patterning lithography** [7973-18]
H. Zhang, Y. Du, M. D. F. Wong, Univ. of Illinois at Urbana-Champaign (United States); R. Topaloglu, GlobalFoundries Corp. (United States); W. Conley, Freescale Semiconductor Corp. (United States)

DOUBLE PATTERNING II

- 7973 OK **Mandrel-based patterning: density multiplication techniques for 15nm nodes (Invited Paper)** [7973-19]
C. Bencher, H. Dai, L. Miao, Y. Chen, P. Xu, Y. Chen, S. Oemardani, Applied Materials, Inc. (United States); J. Sweis, Cadence Design Systems, Inc. (United States); V. Wiaux, J. Hermans, IMEC (Belgium); L.-W. Chang, X. Bao, H. Yi, H.-S. P. Wong, Stanford Univ. (United States)
- 7973 OL **Characterization of a 'thermal freeze' litho-litho-etch (LLE) process for predictive simulation** [7973-20]
S. A. Robertson, KLA-Tencor Corp. (United States); P. Wong, IMEC (Belgium); J. J. Biafore, M. D. Smith, KLA-Tencor Corp. (United States); N. Vandenbroeck, V. Wiaux, IMEC (Belgium)
- 7973 OM **Improving double patterning flow by analyzing the diffractive orders in the pupil plane** [7973-21]
N. Zeggaoui, STMicroelectronics (France) and CNRS-LTM (France); V. Farys, STMicroelectronics (France); M. Besacier, CNRS-LTM (France); Q. Li, Mentor Graphics (United States); E. Yesilada, STMicroelectronics (France); Y. Trouiller, STMicroelectronics (France) and CEA-LETI (France)
- 7973 ON **Spacer-defined double patterning for 20nm and beyond logic BEOL technology** [7973-22]
R. Kim, GLOBALFOUNDRIES Inc. (United States); C. Koay, S. D. Burns, Y. Yin, J. C. Arnold, C. Waskiewicz, S. Mehta, M. Burkhardt, M. E. Colburn, IBM Research (United States); H. J. Levinson, GLOBALFOUNDRIES Inc. (United States)

MASK 3D MODELING

- 7973 OO **Accuracy and performance of 3D mask models in optical projection lithography** [7973-23]
V. Agudelo, Graduate School of Advanced Optical Technologies (Germany), Friedrich-Alexander-Univ. Erlangen-Nürnberg (Germany), and Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany); P. Evanschitzky, A. Erdmann, T. Fühner, Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany); F. Shao, Erlangen Graduate School of Advanced Optical Technologies (Germany) and Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany); S. Limmer, D. Fey, Friedrich-Alexander-Univ. Erlangen-Nürnberg (Germany)
- 7973 OP **Accounting for mask topography effects in source-mask optimization for advanced nodes** [7973-24]
T. H. Coskun, Cadence Design Systems (United States); H. Dai, Applied Materials, Inc. (United States); H.-T. Huang, V. Kamat, Cadence Design Systems (United States); C. Ngai, Applied Materials, Inc. (United States)

TOOLS AND PROCESS CONTROL I

- 7973 OQ **Improved fab CDU with FlexRay and LithoTuner** [7973-25]
R. Socha, ASML (United States); W. Shao, X. Xie, Brion Technologies (United States); Y. van Dommelen, ASML (United States); D. Oorschot, H. Megens, ASML (Netherlands); V. Vellanki, Brion Technologies (United States)

- 7973 OR **Optical proximity stability control of ArF immersion clusters** [7973-26]
L. Van Look, J. Bekaert, K. D'havé, B. Laenens, G. Vandenberghe, S. Cheng, IMEC (Belgium); K. Schreel, J.-W. Gemmink, ASML (Netherlands)
- 7973 OS **Scanner matching using pupil intensity control between scanners in 30nm DRAM device** [7973-27]
J. Jang, D. Park, J. Choi, A. Jung, G. Yoo, J. Kim, C. Kim, D. Yim, Hynix Semiconductor Inc. (Korea, Republic of); J. Lu, S. Park, Z. Yu, V. Vellanki, W. Shao, Brion Technologies, Inc. (United States); C. Park, ASML (Korea, Republic of)
- 7973 OT **Enabling 22-nm logic node with advanced RET solutions** [7973-68]
V. Farys, STMicroelectronics (France); L. Depre, Brion Technologies (United States); J. Finders, ASML Netherlands B.V. (Netherlands); V. Arnoux, Brion Technologies (United States); Y. Trouiller, STMicroelectronics (France); H. Y. Liu, Brion Technologies (United States); E. Yesilada, N. Zeggaoui, C. Alleaume, STMicroelectronics (France)

TOOLS AND PROCESS CONTROL II

- 7973 OU **Solutions for 22-nm node patterning using ArF_i technology** [7973-29]
J. Finders, M. Dusa, J. Mulken, ASML (Netherlands); Y. Cao, Brion Technologies, Inc. (United States); M. Escalante, ASML (Netherlands)
- 7973 OV **Characterization and control of dynamic lens heating effects under high volume manufacturing conditions** [7973-30]
J. Bekaert, L. Van Look, G. Vandenberghe, IMEC (Belgium); P. van Adrichem, ASML (Netherlands) and Brion Technologies (United States); M. J. Maslow, J. -W. Gemmink, ASML (Netherlands); H. Cao, S. Hunsche, Brion Technologies (United States); J. T. Neumann, A. Wolf, Carl Zeiss SMT GmbH (Germany)
- 7973 OW **An aberration control of projection optics for multi-patterning lithography** [7973-31]
Y. Ohmura, T. Ogata, T. Hirayama, H. Nishinaga, T. Shiota, S. Ishiyama, S. Isago, H. Kawahara, T. Matsuyama, Nikon Corp. (Japan)

COMPUTATIONAL LITHOGRAPHY

- 7973 OX **Fine calibration of physical resist models: the importance of Jones pupil, laser bandwidth, mask error and CD metrology for accurate modeling at advanced lithographic nodes** [7973-32]
S. Moon, S. Yang, A. Shamsuarov, E. Kim, J. Ser, Y. Kim, S. Choi, C. Kang, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); U. Klostermann, B. Kchler, Synopsys Inc. (Germany); J. Lewellen, Synopsys, Inc. (United States); T. Schmller, Synopsys Inc. (Germany); S. Lee, Synopsys Inc. (Korea, Republic of)

INNOVATIVE LITHOGRAPHY PROCESS CONTROL: JOINT SESSION WITH CONFERENCE 7971

- 7973 OZ **Stability and calibration of overlay and focus control for a double patterning immersion scanner** [7973-34]
M. Yasuda, S. Wakamoto, H. Imagawa, S. Takubo, Y. Shiba, T. Kikuchi, Y. Shirata, Y. Ishii, Nikon Corp. (Japan)

- 7973 10 **Advanced CDU improvement for 22nm and below** [7973-35]
T. Fujiwara, T. Toki, D. Tanaka, J. Kosugi, T. Susa, N. Sakasai, A. Tokui, Nikon Corp. (Japan)
- 7973 11 **Combined overlay, focus and CD metrology for leading edge lithography** [7973-36]
M. Ebert, H. Cramer, W. Tel, M. Kubis, H. Megens, ASML (Netherlands)
- 7973 12 **Correcting image placement errors using registration control (RegC) technology** [7973-37]
E. Graitzer, Carl Zeiss SMS (Israel); G. Antesberger, Advanced Mask Technology Ctr. (Germany); G. Ben-Zvi, A. Cohen, V. Dmitriev, Carl Zeiss SMS (Israel); S. Winkelmeier, Advanced Mask Technology Ctr. (Germany)

MASK AND LAYOUT OPTIMIZATION

- 7973 14 **Optical lithography applied to 20-nm CMOS Logic and SRAM** [7973-39]
V. Axelrad, Sequoia Design Systems, Inc. (United States); M. C. Smayling, Tela Innovations, Inc. (United States); K. Tsujita, K. Takahashi, Canon Inc. (Japan)
- 7973 15 **3D lithography modeling for ground rule development** [7973-40]
C. Sarma, Infineon Technologies (United States); T. Bailey, A. Lyons, D. Shao, IBM Microelectronics (United States)
- 7973 16 **Mask enhancer technology with source mask optimization (SMO) for 2Xnm-node logic layout gate fabrication** [7973-41]
T. Matsuda, S. Irie, T. Shimizu, T. Yuito, Y. Tabata, Y. Nonami, A. Misaka, T. Koizumi, M. Sasago, Panasonic Corp., Semiconductor Co. (Japan)
- 7973 17 **Evaluation of a new model of mask topography effects** [7973-42]
C. Pierrat, IC Images Technologies (United States)
- 7973 18 **High-performance intensity slope correction method for global process variability band improvement and printability enhancement in RET applications** [7973-43]
S. M. Komirenko, Mentor Graphics Corp. (United States)

OPTICAL/DFM: JOINT SESSION WITH CONFERENCE 7974

- 7973 19 **Contact patterning strategies for 32-nm and 28-nm technology** [7973-44]
B. Morgenfeld, I. Stobert, J. An, IBM Semiconductor Research and Development Ctr. (United States); H. Kanai, Toshiba America Electronic Components, Inc. (Japan); N. Chen, GLOBALFOUNDRIES Inc. (United States); M. Aminpur, C. Brodsky, A. Thomas, IBM Semiconductor Research and Development Ctr. (United States)

SOURCE AND MASK OPTIMIZATION II

- 7973 1A **Polarization holograms for source-mask optimization** [7973-45]
T. D. Milster, H. Noble, E. Ford, W. Dallas, R. A. Chipman, College of Optical Sciences, The Univ. of Arizona (United States); I. Matsubara, Y. Unno, Canon U.S.A., Inc. (United States); S. McClain, P. Khulbe, W. S. T. Lam, D. Hansen, College of Optical Sciences, The Univ. of Arizona (United States)

- 7973 1B **Extending SMO into the lens pupil domain** [7973-46]
M. Kempell Sears, G. Fenger, J. Mailfert, B. Smith, Rochester Institute of Technology (United States)
- 7973 1C **Enhancing fullchip ILT mask synthesis capability for IC manufacturability** [7973-47]
T. Cecil, C. Ashton, D. Irby, L. Luan, D. H. Son, G. Xiao, X. Zhou, D. Kim, B. Gleason, Luminescent Technologies, Inc. (United States); H. J. Lee, W. J. Sim, M. J. Hong, S. G. Jung, S. S. Suh, S. W. Lee, Samsung Electronics (Korea, Republic of)
- 7973 1E **A study of source mask optimization for logic device through experiment and simulations** [7973-49]
H. Kim, J. Lee, J.-C. Shin, Y.-K. Bae, S. Choi, H.-Y. Kang, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

TOOLS

- 7973 1F **Practical performance and enabling technologies in immersion scanners for the double patterning generation** [7973-50]
J. Ishikawa, H. Kohno, S. Sato, J. Kosugi, Y. Shibazaki, Nikon Corp. (Japan)
- 7973 1G **Advanced wavefront engineering for improved imaging and overlay applications on a 1.35 NA immersion scanner** [7973-51]
F. Staals, A. Andryzhieuskaya, H. Bakker, M. Beems, J. Finders, T. Hollink, J. Mulken, A. Nachtwein, R. Willekers, ASML Netherlands B.V. (Netherlands); P. Engblom, ASML Boise (United States); T. Gruner, Carl Zeiss SMT AG (Germany); Y. Zhang, Brion Technologies, Inc. (United States)
- 7973 1H **Pupilgram adjusting scheme using intelligent illuminator for ArF immersion exposure tool** [7973-52]
T. Matsuyama, N. Kita, Y. Mizuno, Nikon Corp. (Japan)
- 7973 1I **Scanner matching for standard and freeform illumination shapes using FlexRay** [7973-53]
J. Bekaert, L. Van Look, K. D'havé, B. Laenens, G. Vandenberghe, IMEC (Belgium); P. van Adrichem, Brion Technologies (United States) and ASML (Netherlands); W. Shao, J. Ghan, Brion Technologies (United States); K. Schreel, ASML (Netherlands); J. T. Neumann, Carl Zeiss SMT GmbH (Germany)
- 7973 1K **Ecology and high-durability injection locked laser with flexible power for double-patterning ArF immersion lithography** [7973-55]
H. Umeda, H. Tsushima, H. Watanabe, S. Tanaka, M. Yoshino, S. Matsumoto, H. Tanaka, A. Kurosu, Y. Kawasuji, T. Matsunaga, J. Fujimoto, H. Mizoguchi, Gigaphoton Inc. (Japan)

Part Two

POSTER SESSION: COMPUTATIONAL LITHOGRAPHY

- 7973 1L **Hotspot fixing using ILT** [7973-56]
W. Sim, S. Jung, H.-J. Lee, S. Suh, J. Ser, S.-W. Choi, C.-J. Kang, SAMSUNG Electronics (Korea, Republic of); T. Cecil, C. Ashton, D. Irby, X. Zhou, D. H. Son, G. Xiao, D. Kim, Luminescent Technologies, Inc. (United States)
- 7973 1M **Fast algorithm for quadratic aberration model based on cross triple correlation** [7973-57]
W. Liu, T. Zhou, S. Liu, Huazhong Univ. of Science and Technology (China)
- 7973 1N **Choosing objective functions for inverse lithography patterning** [7973-58]
J.-C. Yu, P. Yu, National Chiao Tung Univ. (Taiwan)
- 7973 1O **Physical conversion of Stokes parameters which are multiplied by a general Mueller matrix into Jones vectors applicable to the lithographic calculation** [7973-59]
H. Nomura, M. Takahashi, S. Kyoh, Toshiba Corp. (Japan)

POSTER SESSION: DOUBLE PATTERNING

- 7973 1P **Self-aligned triple patterning for continuous IC scaling to half-pitch 15nm** [7973-60]
Y. Chen, P. Xu, L. Miao, Y. Chen, X. Xu, D. Mao, P. Blanco, C. Bencher, R. Hung, C. S. Ngai, Applied Materials, Inc. (United States)
- 7973 1Q **Sidewall spacer quadruple patterning for 15nm half-pitch** [7973-61]
P. Xu, Y. Chen, Y. Chen, L. Miao, S. Sun, S. Kim, Applied Materials, Inc. (United States); A. Berger, Applied Materials, Inc. (Israel); D. Mao, C. Bencher, R. Hung, C. Ngai, Applied Materials, Inc. (United States)
- 7973 1R **Spacer defined double patterning for (sub-)20nm half pitch single damascene structures** [7973-62]
J. Versluijs, Y. K. Siew, E. Kunnen, D. Vangoidsenhoven, S. Demuynck, V. Wiaux, H. Dekkers, G. Beyer, IMEC (Belgium)
- 7973 1S **Recessive self-aligned double patterning with gap-fill technology** [7973-63]
Y. Chen, X. Xu, Y. Chen, L. Miao, H. Chen, P. Blanco, C. S. Ngai, Applied Materials, Inc. (United States)
- 7973 1T **Spatial frequency multiplication techniques towards half-pitch 10nm patterning** [7973-64]
Y. Chen, Y. Chen, L. Miao, P. Xu, X. Xu, H. Chen, P. Blanco, R. Hung, C. S. Ngai, Applied Materials, Inc. (United States)

POSTER SESSION: FREEFORM AND SMO

- 7973 1U **Influence of the illumination source on model-based SRAF placement** [7973-65]
R. Gupta, A. Dave, E. Tejnil, S. Jayaram, P. LaCour, Mentor Graphics Corp. (United States)
- 7973 1V **Comparison of clear-field and dark-field images with optimized masks** [7973-66]
R. Sinn, T. Dam, B. Gleason, Luminescent Technologies (United States)

- 7973 1W **Custom source and mask optimization for 20nm SRAM and logic** [7973-67]
M. C. Smayling, Tela Innovations, Inc. (United States); T. H. Coskun, V. Kamat, Cadence Design Systems, Inc. (United States)
- 7973 1X **Improvement of lithography process by using a FlexRay illuminator for memory applications** [7973-69]
T. Huang, C.-Y. Huang, Nanya Technology Corp. (Taiwan); T.-B. Chiou, ASML Technology Development Ctr. (Taiwan); M. Hsu, ASML Strategic Marketing (Taiwan); C.-L. Shih, Nanya Technology Corp. (Taiwan); A. Chen, ASML Technology Development Ctr. (Taiwan); M.-K. Wei, Nanya Technology Corp. (Taiwan)
- 7973 1Y **Quantification of the difference between two sources by Zernike polynomial decomposition** [7973-70]
C. Alleaume, E. Yesilada, V. Farys, STMicroelectronics (France); Y. Trouiller, CEA-LETI (France)
- 7973 1Z **A simple method of source optimization for advanced NAND FLASH process** [7973-71]
Y.-S. Chang, Powerchip Technology Corp. (Taiwan); S. Ogasawara, K. Fujii, S. Hirukawa, M. Imai, Nikon Corp. (Japan); W.-L. Kuo, C.-C. Lin, Powerchip Technology Corp. (Taiwan)
- 7973 20 **Gradient-based fast source mask optimization (SMO)** [7973-72]
J.-C. Yu, P. Yu, National Chiao Tung Univ. (Taiwan)
- 7973 21 **Beam shaping: top hat and customized intensity distributions for semiconductor manufacturing and inspection** [7973-73]
A. Teipel, L. Aschke, LIMO Lissotschenko Mikrooptik GmbH (Germany)
- 7973 22 **Source and mask optimization applications in manufacturing** [7973-74]
C. Lim, V. Temchenko, Infineon Technologies Dresden GmbH (Germany); U. Klostermann, V. Domnenko, Synopsys, Inc. (Germany); J. Schneider, D. Sarlette, I. Meusel, D. Kaiser, Infineon Technologies Dresden GmbH (Germany); R. Ploss, Toppan Photomasks Germany GmbH (Germany)
- 7973 23 **Hierarchical kernel generation for SMO application** [7973-75]
J. H.-C. Chang, C. C.-P. Chen, National Taiwan Univ. (Taiwan); L. Melvin III, Synopsys Inc. (Taiwan)

POSTER SESSION: LASER

- 7973 26 **High-range laser light bandwidth measurement and tuning** [7973-78]
K. O'Brien, R. Jiang, N. Han, E. Figueroa, R. Rao, R. J. Rafac, Cymer, Inc. (United States)
- 7973 27 **DUV light source availability improvement via further enhancement of gas management technologies** [7973-79]
D. J. Riggs, K. O'Brien, D. J. W. Brown, Cymer, Inc. (United States)

POSTER SESSION: SCANNER-LITHOGRAPHY OPTIMIZATION

- 7973 28 **Focus drilling for increased process latitude in high-NA immersion lithography** [7973-80]
I. Lalovic, J. Lee, N. Seong, N. Farrar, Cymer, Inc. (United States); M. Kupers, Cymer B.V.

- (Netherlands); H. van der Laan, T. van der Hoeff, C. Kohler, ASML (Netherlands)
- 7973 29 **Compensation of mask induced aberrations by projector wavefront control** [7973-81]
P. Evanschitzky, Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany); F. Shao, Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany) and Erlangen Graduate School of Advanced Optical Technologies (Germany); T. Fühner, Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany); A. Erdmann, Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany) and Erlangen Graduate School of Advanced Optical Technologies (Germany)
- 7973 2A **Advanced scanner matching using freeform source and lens manipulators** [7973-82]
J.-H. Lim, K. Kang, S.-M. Kim, SAMSUNG Semiconductor (Korea, Republic of); W. Shao, F. Du, Z. Zhang, Z. Yu, J. Barbuto, V. Vellanki, Y. Cao, R. Goossens, Brion Technologies, Inc. (United States); S.-H. Park, C. K. Park, S. Hunsche, ASML Korea Co., Ltd. (Korea, Republic of); J. Lu, Brion Technologies Co., Ltd. (China)
- 7973 2B **Measurement of wavefront distortions in DUV optics due to lens heating** [7973-83]
K. Mann, A. Bayer, U. Leinhos, M. Schöneck, B. Schäfer, Laser-Lab. Göttingen e.V. (Germany)
- 7973 2C **Improved immersion scanning speed using superhydrophobic surfaces** [7973-84]
A. K. Gnanappa, E. Gogolides, NCSR Demokritos (Greece); E. Feuillet, F. Evangelista, N. Dziomkina, M. Riepen, ASML (Netherlands)
- 7973 2D **New 0.75 NA ArF scanning lithographic tool** [7973-85]
L. Duan, J. Cheng, G. Sun, Y. Chen, Shanghai Micro Electronics Equipment Co., Ltd. (China)
- 7973 2E **Simulation-based scanner tuning using FlexRay capability and scatterometry** [7973-111]
K. Bubke, GLOBALFOUNDRIES (Germany); M. Ruhm, ASML (Netherlands); R. Aldana, M. Niehoff, X. Xie, J. Ghan, Brion Technologies, Inc. (United States); P. van Adrichem, ASML (Germany); H. Bald, GLOBALFOUNDRIES (Germany); P. Luehrmann, ASML (Netherlands); S. Roling, R. Seltmann, GLOBALFOUNDRIES (Germany)

POSTER SESSION: MASK/WAFER TOPOGRAPHY, LAYOUT, AND OPC

- 7973 2F **Investigating the performance of directional boundary layer model through staged modeling method** [7973-87]
M.-G. Jeong, W.-C. Lee, S.-H. Yang, S.-H. Jang, S.-B. Shim, Y.-C. Kim, C. Suh, S.-W. Choi, Y.-H. Kim, SAMSUNG Electronics (Korea, Republic of)
- 7973 2G **Large scale model of wafer topography effects** [7973-88]
N. Voznesenskiy, Synopsys, Inc. (Estonia); H.-J. Stock, B. Küchler, Synopsys GmbH (Germany); H. Song, J. Shiely, Synopsys, Inc. (United States); L. Bomholt, Synopsys Switzerland, LLC (Switzerland)
- 7973 2H **Study of model assisted rule base SRAF for random contact** [7973-89]
J. Moon, B.-S. Nam, C.-K. Kim, H.-S. Yun, Hynix Semiconductor Inc. (Korea, Republic of); J.-Y. Lee, Mentor Graphics (Korea, Republic of); D. Yim, S.-K. Park, Hynix Semiconductor Inc. (Korea, Republic of)
- 7973 2I **Physical simulation for verification and OPC on full chip level** [7973-90]
S. Shim, S. Moon, Y. Kim, S. Choi, Y. Kim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of);

B. Kchler, U. Klostermann, Synopsys GmbH (Germany); M. Do, S. Lee, Synopsys Korea Inc. (Korea, Republic of)

- 7973 2J **Mask data correction methodology in the context of model-based fracturing and advanced mask models** [7973-91]
C. Pierrat, IC Images Technologies, Inc. (United States); L. Chau, I. Bork, D2S, Inc. (United States)
- 7973 2K **Optimizing OPC data sampling based on "orthogonal vector space"** [7973-92]
Y. Sun, Y. M. Foong, Y. Wang, J. Cheng, D. Zhang, S. Gao, N. Chen, B. I. Choi, GLOBALFOUNDRIES (Singapore); A. J. Bruguier, M. Feng, J. Qiu, S. Hunsche, L. Liu, W. Shao, Brion Technologies, Inc. (United States)
- 7973 2M **Tolerance-based OPC and solution to MRC-constrained OPC** [7973-94]
Y. Ping, X. Li, S. Jang, D. Kwa, Y. Zhang, R. Lugg, Synopsys, Inc. (United States)
- 7973 2N **Study of various RET for process margin improvement in 3X-nm DRAM contact** [7973-95]
H. Sim, H. Yune, Y. Ahn, J. Moon, B. Nam, D. Yim, S. Park, Hynix Semiconductor Inc. (Korea, Republic of)
- 7973 2O **A cost-driven fracture heuristics to minimize external sliver length** [7973-96]
X. Ma, S. Jiang, A. Zakhor, Univ. of California, Berkeley (United States)
- 7973 2P **A recursive cost-based approach to fracturing** [7973-97]
S. Jiang, X. Ma, A. Zakhor, Univ. of California, Berkeley (United States)
- 7973 2R **Full-chip OPC and verification with a fast mask 3D model** [7973-99]
H.-T. Huang, A. Mokhberi, Cadence Design Systems, Inc. (United States); H. Dai, C. Ngai, Applied Materials, Inc. (United States)
- 7973 2S **Overcome the process limitation by using inverse lithography technology with assist feature** [7973-100]
Y.-A. Shim, S. Jun, J. Choi, K. Choi, J. Han, Dongbu HiTek Co., Ltd. (Korea, Republic of); K. Wang, J. McCarthy, G. Xiao, G. Dai, D. Son, X. Zhou, T. Cecil, D. Kim, K. Baik, Luminescent Technology (United States)
- 7973 2T **Improvement on post-OPC verification efficiency for contact/via coverage check by final CD biasing of metal lines and considering their location on the metal layout** [7973-101]
Y. Kim, J.-Y. Choi, K. Choi, Dongbu HiTek (Korea, Republic of); J.-H. Choi, S.-R. Lee, Synopsys Inc. (Korea, Republic of)

POSTER SESSION: MODELING

- 7973 2V **Performance of a bilinear photoresist model** [7973-103]
A. Burov, M. Shi, J. Yan, W. Sun, Shanghai Micro Electronics Equipment Co., Ltd. (China)
- 7973 2W **Application of an inverse Mack model for negative tone development simulation** [7973-104]
W. Gao, Synopsys GmbH (Germany) and IMEC (Belgium); U. Klostermann, T. Mlders, T. Schmoeller, W. Demmerle, Synopsys GmbH (Germany); P. De Bisschop, J. Bekaert, IMEC (Belgium)

- 7973 2X **A study of quantum lithography for diffraction limit** [7973-105]
S.-K. Kim, Hanyang Univ. (Korea, Republic of)
- 7973 2Y **Evaluating the performance of DP and EUVL by using analytical equations for resolution of optical lithography with considering required DOF** [7973-106]
M. Shibuya, K. Nogami, Tokyo Polytechnic Univ. (Japan); A. Takada, Topcon Corp. (Japan); S. Nakadate, Tokyo Polytechnic Univ. (Japan)

POSTER SESSION: TOOL AND PROCESS CONTROL

- 7973 2Z **Lithography process control using focus and dose optimisation technique** [7973-108]
N. Spaziani, LTM/CNRS (France) and STMicroelectronics (France); R.-L. Inglebert, LTM/CNRS (France); J. Massin, STMicroelectronics (France)
- 7973 31 **Feasibility study on the mask compensation of gate CD non-uniformity caused by etching process** [7973-110]
W. H. Kim, E. J. Yet, S. I. Yet, B. C. Lee, X-FAB Sarawak Sdn. Bhd. (Malaysia)

Author Index

Conference Committee

Symposium Chairs

Donis G. Flagello, Nikon Research Corporation of America (United States)

Harry J. Levinson, GLOBALFOUNDRIES Inc. (United States)

Conference Chair

Mircea V. Dusa, ASML US, Inc. (United States)

Cochair

Will Conley, Freescale Semiconductor, Inc. (United States)

Program Committee

Pary Baluswamy, Micron Technology, Inc. (United States)

Peter D. Buck, Toppan Photomasks, Inc. (United States)

Andreas Erdmann, Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany)

Nigel R. Farrar, Cymer, Inc. (United States)

Carlos Fonseca, Tokyo Electron America, Inc. (United States)

Soichi Inoue, Toshiba Materials Company, Ltd. (Japan)

Jongwook Kye, GLOBALFOUNDRIES Inc. (United States)

Tsai-Sheng Gau, Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)

Kafai Lai, IBM Corporation (United States)

Sukjoo Lee, SAMSUNG Electronics Company, Ltd. (Korea, Republic of)

Wilhelm Maurer, Infineon Technologies AG (Germany)

Soichi Owa, Nikon Corporation (Japan)

Bruce W. Smith, Rochester Institute of Technology (United States)

Kazuhiro Takahashi, Canon Inc. (Japan)

Geert Vandenberghe, IMEC (Belgium)

Sam Sivakumar, Intel Corporation (United States)

Session Chairs

Introduction, Opening Remarks, and Special Recognition

Mircea V. Dusa, ASML US, Inc. (United States)

Will Conley, Freescale Semiconductor, Inc. (United States)

- 1 Invited Session
Mircea V. Dusa, ASML US, Inc. (United States)
Will Conley, Freescale Semiconductor, Inc. (United States)
- 2 FreeForm and SMO
Soichi Inoue, Toshiba Materials Company, Ltd. (Japan)
Sam Sivakumar, Intel Corporation (United States)
- 3 Source and Mask Optimization I
Andreas Erdmann, Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany)
Sukjoo Lee, SAMSUNG Electronics Company, Ltd. (Korea, Republic of)
- 4 Double Patterning I
Carlos Fonseca, Tokyo Electron America, Inc. (United States)
Peter D. Buck, Toppan Photomasks, Inc. (United States)
- 5 Double Patterning II
Jongwook Kye, GLOBALFOUNDRIES Inc. (United States)
Tsai-Sheng Gau, Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)
- 6 Mask 3D Modeling
Peter D. Buck, Toppan Photomasks, Inc. (United States)
Andreas Erdmann, Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany)
- 7 Tools and Process Control I
Kafai Lai, IBM Corporation (United States)
Nigel R. Farrar, Cymer, Inc. (United States)
- 8 Tools and Process Control II
Wilhelm Maurer, Infineon Technologies AG (Germany)
Soichi Owa, Nikon Corporation (Japan)
- 9 Computational Lithography
Soichi Inoue, Toshiba Materials Company, Ltd. (Japan)
Geert Vandenberghe, IMEC (Belgium)
- 10 Innovative Lithography Process Control: Joint Session with Conference 7971
Alexander Starikov, I&I Consulting (United States)
Will Conley, Freescale Semiconductor, Inc. (United States)
- 11 Mask and Layout Optimization
Bruce W. Smith, Rochester Institute of Technology (United States)
Kazuhiro Takahashi, Canon Inc. (Japan)

- 12 Optical/DFM: Joint Session with Conference 7974
 Mircea V. Dusa, ASML US, Inc. (United States)
 Luigi Capodieci, GLOBALFOUNDRIES Inc. (United States)
- 13 Source and Mask Optimization II
 Geert Vandenberghe, IMEC (Belgium)
 Kafai Lai, IBM Corporation (United States)
- 14 Tools
 Sam Sivakumar, Intel Corporation (United States)
 Soichi Owa, Nikon Corporation (Japan)
- Poster Session: Computational Lithography
 Soichi Inoue, Toshiba Materials Company, Ltd. (Japan)
- Poster Session: Double Patterning
 Jongwook Kye, GLOBALFOUNDRIES Inc. (United States)
 Carlos Fonseca, Tokyo Electron America, Inc. (United States)
- Poster Session: FreeForm and SMO
 Sam Sivakumar, Intel Corporation (United States)
 Kafai Lai, IBM Corporation (United States)
- Poster Session: Laser
 Nigel R. Farrar, Cymer, Inc. (United States)
- Poster Session: Scanner-Lithography Optimization
 Pary Baluswamy, Micron Technology, Inc. (United States)
- Poster Session: Mask/Wafer Topography, Layout, and OPC
 Peter D. Buck, Toppan Photomasks, Inc. (United States)
 Bruce W. Smith, Rochester Institute of Technology (United States)
- Poster Session: Modeling
 Andreas Erdmann, Fraunhofer-Institut für Integrierte System und
 Bauelementetechnologie (Germany)
- Poster Session: Tool and Process Control
 Geert Vandenberghe, IMEC (Belgium)