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Advanced Etch Technology for Nanopatterning

**Ying Zhang
Gottlieb Oehrlein
Qinghuang Lin**
Editors

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Introduction

The success of the semiconductor industry has been enabled by the relentless pursuit of technological innovations. The continuous strive to improve device features, enhance performance and simultaneously reduce manufacturing costs is incessant. While optical lithography has traditionally been the major driving force to advance technology, new materials and enhanced synergy between fabrication technologies have become increasingly important for the development of manufacturing at advanced-technology nodes. One such area of increased importance involves plasma etch and related patterning technology. While plasma etch has always been an integral part of semiconductor technology, it has significantly grown in importance with the emergence of Double Patterning and Pitch-Splitting (DP/PS) technology for 22 nm technology node and beyond.

Recent advances in lithographic technology include 193-nm immersion optical lithography, EUV lithography, Multi-e-Beam Direct Writing (MEBDW), and alternative lithographic technologies, such as directed self-assembly patterning (DSA), and nanoimprint lithography. All of these lithography technologies depend on advancing plasma etch, which is used either directly in the patterning process, such as patterning and forming lithography masks, or in transferring lithographic patterns into other layers, e.g. during multi-litho and multi-etching lithography patterning, which will be most likely used for high-volume manufacturing (HVM) at 22nm technology node and beyond. The increasing interactions and inter-dependence of lithography, photoresist technologies, and plasma etch technologies inevitably makes advancing lithography and plasma etch technologies for semiconductor manufacturing more challenging. This situation is the motivation for having an "Advanced Etch Technology for Nanoattenuation Conference (AETNC)" as a key part of the SPIE Advanced Lithography Symposium starting 2012. This new conference brings lithography and plasma-etching communities together to exchange ideas, share new research and development results, discuss gaps in our fundamental understanding and resolve challenges facing the semiconductor industry.

We aim to establish the AETNC as a premier and influential conference on plasma etch technology in the semiconductor industry and to complement the technical programs of other conferences at the SPIE Advanced Lithography Symposium. The first AETNC featured papers from major integrated device manufacturers (IDM's), foundries, key tool vendors, research institutes, national labs, and universities from around the world. These papers covered all key aspects related to plasma etching for advanced patterning technologies for Logic and Memory products, FEOL applications (such as the formation of 3D device structures of FinFET, BEOL challenges and possible solutions line-edge roughness (LER) for a variety of resists, e.g., 193i, EUV, e-beam resists, etc.), wet etch, resist stripping, and UV treatment/processing. Topics related to key emerging technologies for

nanopatterning, such as directed self-assembly (DSA), were also presented during the conference.

This proceedings volume collects selected papers presented at the first AETNC, held on February 13–14th, 2012 as part of the SPIE Advanced Lithography Symposium 2012.

We would like to take this opportunity to thank the SPIE 2012 Advanced Lithography Symposium Committee for helping initiate the AETNC. The dedication, enthusiasm, and efforts of many committee members, keynote speakers, invited speakers, and authors of contributed papers of AETNC made this conference success. Please accept our well-deserved thanks!

Ying Zhang
Gottlieb Oehrlein
Qinghuang Lin