# Contents

<table>
<thead>
<tr>
<th>Page</th>
<th>Section</th>
</tr>
</thead>
<tbody>
<tr>
<td>vii</td>
<td>Conference Committee</td>
</tr>
<tr>
<td>ix</td>
<td>Introduction</td>
</tr>
<tr>
<td></td>
<td>SESSION 1 REVIEWS AND OVERVIEWS OF NANOPATTERNING CHALLENGES</td>
</tr>
</tbody>
</table>
| 9054 04 | Patterning challenges in the fabrication of 12 nm half-pitch dual damascene copper ultra low-k interconnects (Invited Paper) [9054-3]  
J. S. Chawla, K. J. Singh, A. Myers, D. J. Michalak, R. Schenker, C. Jezewski, B. Krist,  
F. Gstrein, T. K. Indukuri, H. J. Yoo, Intel Corp. (United States) |
|      | SESSION 2 NANOPATTERNING FOR ADVANCED LOGIC AND MEMORY TECHNOLOGY NODES |
| 9054 05 | Line width roughness reduction strategies for patterns exposed via electron beam lithography [9054-26]  
J. Jussot, Univ. Joseph Fourier (France); E. Pargon, LTM CNRS (France); B. Icard, CEA-LETI (France); J. Bustos, STMicroelectronics (France); L. Pain, CEA-LETI (France) |
| 9054 06 | Effect of etch pattern transfer on local overlay (OVL) margin in 28nm gate integration. [9054-5]  
O. Ros, P. Gouraud, B. Le-Gratiet, C. Gardin, J. Ducoté, STMicroelectronics (France); E. Pargon, LTM CNRS (France) |
| 9054 07 | Gate double patterning strategies for 10nm node FinFET devices [9054-6]  
H. Hody, IMEC (Belgium); V. Paraschiv, SC Etch Tech Solutions (Romania); D. Hellin, LAM Research Corp. (Belgium); T. Vandeweyer, G. Boccardi, K. Xu, IMEC (Belgium) |
| 9054 08 | 28nm FDSOI high-K metal gate CD variability investigation [9054-7]  
L. Desvoivres, CEA-LETI (France); P. Gouraud, B. Le Gratiet, R. Bouyssou, R. Ranica,  
C. Gallon, I. Thomas, STMicroelectronics (France) |
| 9054 09 | Highly selective etch gas chemistry design for precise DSAL dry development process [9054-8]  
M. Omura, T. Imamura, H. Yamamoto, I. Sakai, H. Hayashi, Toshiba Corp. (Japan) |
|      | SESSION 3 PLASMA AND RESIST INTERACTIONS, INCLUDING PATTERNING QUALITY CONTROL (LER, CD UNIFORMITY, ETC.) |
| 9054 OC | Hydrogen plasma treatment: the evolution of roughness in frequency domain [9054-11]  
P. De Schepper, IMEC (Belgium) and Katholieke Univ. Leuven (Belgium); A. Vaglio Pret,  
IMEC (Belgium) and KLA-Tencor Corp. (Belgium); E. Altamirano-Sánchez, IMEC (Belgium);  
Z. el Otell, S. De Gendt, IMEC (Belgium) and Katholieke Univ. Leuven (Belgium) |

---

Proceedings of SPIE Vol. 9054 905401-3  
Downloaded From: https://www.spiedigitallibrary.org/conference-proceedings-of-spie on 24 Apr 2020  
Terms of Use: https://www.spiedigitallibrary.org/terms-of-use
SESSION 4  PATTERNING INTEGRATION SCHEMES (MULTILAYER PATTERNING, SELF-ALIGNED PATTERNING, ETC.)

9054 0E  Plasma etching and integration challenges using alternative patterning techniques for 11nm node and beyond (Invited Paper) [9054-13]
S. Barnola, P. Pimenta Barros, CEA-LETI (France); C. Arvet, STMicroelectronics (France); C. Vizioz, N. Posseme, A. Gharbi, M. Argoud, R. Tiron, J. Pradelles, L. Desvoivres, S. Barraud, CEA-LETI (France)

9054 0G  Etch challenges for DSA implementation in CMOS via patterning [9054-15]
P. Pimenta Barros, S. Barnola, A. Gharbi, M. Argoud, I. Servin, R. Tiron, CEA-LETI (France); X. Chevalier, C. Navarro, C. Nicolet, Arkema S.A. (France); C. Lapeyre, CEA-LETI (France); C. Monget, STMicroelectronics (France); E. Martinez, CEA-LETI (France)

SESSION 5  NEW PLASMA SOURCES AND NEW ETCHING TECHNOLOGIES

9054 0H  Large-radius neutral beam enhanced chemical vapor deposition process for non-porous ultra-low-k SiOCH (Invited Paper) [9054-16]
Y. Kikuchi, Tokyo Electron Ltd. (Japan) and Tohoku Univ. (Japan); Y. Sakakibara, Tokyo Electron Ltd. (Japan); S. Samukawa, Tohoku Univ. (Japan)

9054 0I  Precision integrated thickness control with gas cluster ion beam etch (Invited Paper) [9054-17]
N. M. Russell, V. Gizzo, J. D. LaRose, B. D. Pfeiffer, TEL Epion Inc. (United States); R. Dasaka, L. Economikos, R. Wise, IBM Systems and Technology Group (United States)

9054 0K  Advanced plasma sources for the future 450mm etch process [9054-19]
Y. S. Lee, J. W. Lee, G. J. Park, H. Y. Chang, KAIST (Korea, Republic of)

SESSION 6  EMERGING PATTERNING TECHNOLOGIES (DSA AND OTHERS)

9054 0M  A comparison of the pattern transfer of line-space patterns from graphoepitaxial and chemoepitaxial block co-polymer directed self-assembly (Invited Paper) [9054-21]
D. B. Millward, G. S. Lugani, R. Khurana, S. L. Light, Micron Technology, Inc. (United States); A. Niroomand, Micron Technology, Inc. (Belgium); P. D. Hustad, P. Trefonas, S.-W. Chang, C. N. Lee, D. Quach, Dow Electronic Materials (United States)

9054 0O  Directed self-assembly of PS-b-PDMS into 193nm photoresist patterns and transfer into silicon by plasma etching [9054-23]
POSTER SESSION

9054 0P Litho resist rework influences on Cu metal layer patterning with TiN-hard mask [9054-24]
M. Dankelmann, M. Czekalla, H. Estel, J. Hahn, B. K. Hong, M. Lamm, E. Neubert, M. Renner,
R. Scheibel, M. Stegemann, J. Schneider, Infineon Technologies Dresden GmbH (Germany)

9054 0Q Spin-on carbon using fullerene derivatives [9054-25]
A. Frommhold, Univ. of Birmingham (United Kingdom); A. G. Brown, Irresistible Materials Ltd.
(United Kingdom); T. Lada, Nano-C, Inc. (United States); R. E. Palmer, A. P. G. Robinson,
Univ. of Birmingham (United Kingdom)

9054 0R Dual frequency mid-gap capacitively coupled plasma (m-CCP) for conventional and DSA
patterning at 10nm node and beyond [9054-27]
N. Mohanty, A. Ko, C. Cole, V. Rastogi, K. Kumar, TEL Technology Ctr., America, LLC (United
States); G. Schmid, R. Farrell, T. Ryan, E. Hosler, J. Xu, M. Preil, GLOBALFOUNDRIES, Inc.
(United States)

Author Index
Conference Committee

Symposium Chair

Harry J. Levinson, GLOBALFOUNDRIES, Inc. (United States)

Symposium Co-chair

Mircea V. Dusa, ASML US, Inc. (United States)

Conference Chair

Gottlieb S. Oehrlein, University of Maryland, College Park (United States)

Conference Co-chair

Qinghuang Lin, IBM Thomas J. Watson Research Center (United States)

Conference Program Committee

Julie Bannister, Tokyo Electron America, Inc. (United States)
Charles T. Black, Brookhaven National Laboratory (United States)
Maxime Darnon, LTM CNRS (France)
Sebastian U. Engelmann, IBM Thomas J. Watson Research Center (United States)
Eric A. Hudson, LAM Research Corporation (United States)
Catherine B. Labelle, GLOBALFOUNDRIES Inc. (United States)
Nae-Eung Lee, Sungkyunkwan University (Korea, Republic of)
Erwine Pargon, LTM CNRS (France)
Ricardo Ruiz, HGST (United States)
Seiji Samukawa, Tohoku University (Japan)
Denis Shamiryan, MAPPER Lithography B.V. (Netherlands)
Rich Wise, IBM Corporation (United States)
Anthony Yen, TSMC Taiwan (Taiwan)
Ying Zhang, Applied Materials, Inc. (United States)
Jeff Xu, Qualcomm Technologies Inc. (United States)

Session Chairs

1 Reviews and Overviews of Nanopatterning Challenges
   Cathy Labelle, GLOBALFOUNDRIES Inc. (United States)
   Rich Wise, IBM Corporation (United States)
2 Nanopatterning for Advanced Logic and Memory Technology Nodes
Denis Shamiryan, MAPPER Lithography (Netherlands)
Eric A. Hudson, LAM Research Corporation (United States)

3 Plasma and Resist Interactions, Including Patterning Quality Control (LER, CD Uniformity, etc.)
Sebastian U. Engelmann, IBM Thomas J. Watson Research Center (United States)

4 Patterning Integration Schemes (multilayer patterning, self-aligned patterning, etc.)
Maxime Darnon, LTM CNRS (France)
Nae-Eung Lee, Sungkyunkwan University (Korea, Republic of)

5 New Plasma Sources and New Etching Technologies
Seiji Samukawa, Tohoku University (Japan)
Julie Bannister, Tokyo Electron America, Inc. (United States)

6 Emerging Patterning Technologies (DSA and others)
Ying Zhang, Applied Materials, Inc. (Taiwan)
Ricardo Ruiz, HGST (United States)
Introduction

This proceedings volume contains selected papers presented at the conference Advanced Etch Technology for Nanopatterning III held February 24-25, 2014 as part of the SPIE Advanced Lithography Symposium 2014. The meeting featured six sessions of oral presentations to highlight important achievements and challenges in the following areas of Advanced Etch Technology for Nanopatterning:

Session 1: Reviews and Overviews of Nanopatterning Challenges
Session 2: Nanopatterning for Advanced Logic and Memory Technology Nodes
Session 3: Plasma and Resist Interactions, Including Patterning Quality Control (LER, CD Uniformity, etc.)
Session 4: Patterning Integration Schemes (multilayer patterning, self-aligned patterning, etc.)
Session 5: New Plasma Sources and New Etching Technologies
Session 6: Emerging Patterning Technologies (DSA and others)

Additionally, there was a poster session.

We would like to thank all speakers and presenters for their stimulating contributions to the conference. We also would like to express our gratitude to the SPIE Advanced Lithography “Advanced Etch Technology for Nanopatterning III” Conference Committee members for their contributions in organizing this very successful conference. Finally, we would like to thank SPIE and its staff for support of this conference and their arrangements.

Gottlieb S. Oehrlein
Qinghuang Lin