INTRODUCTION TO
Semiconductor Manufacturing Technology

SECOND EDITION

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This textbook is dedicated to my wife, Liu Huang, and my sons, Jarry Xiao and Colin Xiao.

Contents

Preface to the First Edition

The semiconductor industry is developing rapidly with new technology introduced almost on a daily basis. The device feature size is shrinking continuously and the number of transistors on an integrated circuit (IC) chip is increasing rapidly, as predicted by Moore's law. Compared with only a decade ago, IC fabrication processing technology has become more complicated.

This book thoroughly describes the complicated IC chip manufacturing processes in a semiconductor fab, using minimum mathematics, chemistry, and physics. It covers the advanced technologies while keeping the contents simple and easy to understand for readers without science and engineering degrees. It focuses on the newest IC fabrication technologies and describes the older technologies to provide better understanding of the historical development. The processes chosen for the book are very close to those used in real fabs, especially process troubleshooting and process and hardware relations.

This book is intended for technical and college students who need an in-depth understanding of the technology as they prepare to find a job in the field. It is also intended as a reference book for engineering students and to provide a more realistic picture of the semiconductor industry. Industry operators, technicians, engineers, and personnel in sales, marketing, administration, and management can also benefit. This book can help them to learn more about their jobs, improve their troubleshooting and problem-solving skills, and raise their career development potential.

Chapter 1 briefly reviews the history of the semiconductor industry and describes semiconductor manufacturing processes. Chapter 2 introduces basic semiconductor fabrication including yield, cleanroom, semiconductor fab, and IC chip test and packaging. Chapter 3 gives a brief review of fabrication semiconductor devices, IC chips, and early technologies in semiconductor processing. Crystal structure, single-crystal silicon wafer manufacturing, and epitaxial silicon growth are described in Chapter 4. Chapter 5 lists and discusses thermal processes, including oxidation, diffusion, annealing, alloying, and reflow processes. Rapid thermal processes (RTPs) and conventional furnace thermal processes are discussed. Chapter 6 details the photolithography process. Fundamentals of plasmas used in semiconductor processing are covered in Chapter 7, which introduces plasma applications, DC bias, and plasma-process relations. Chapter 8 discusses the ion implantation process. Chapter 9 gives a detailed description of etch processes including wet and dry etches; chemical, reactive ion etch (RIE), and

physical etches; and patterned and blanket etch processes. Basic chemical vapor deposition (CVD) and dielectric thin-film deposition processes, including dielectric CVD processes, process trends, troubleshooting, and future trends are discussed in detail in Chapter 10. Chapter 11 covers metallization, metal CVD, and physical vapor deposition (PVD) processes. It also describes the copper metallization process. Planarization processes including chemical mechanical polishing (CMP) are discussed in Chapter 12. Chapter 13 discusses process integration. Chapter 14 diagrams CMOS process flows including an advanced CMOS process flow with copper and low-κ interconnection. Chapter 15 predicts the future development of the semiconductor industry.

Many people helped me to write this book. I especially appreciate the useful information provided by my current and former colleagues: Lou Frenzel, Thomas E. Thompson, Ole Krogh, Tony Shi, Alberto Quiñonez, Lance Kinney, Scott Bolton, and Steve Reedy. Many of my students helped me by proofreading and improving the book. I especially express my thanks to Wayne Parent, Jeffrey Carroll, Boyd Woods, and Ronald Tabery.

I would also like to thank the following reviewers for their valuable suggestions: Professor Dave Hata, Portland Community College; Professor Fred Lavender, Albuquerque Technical Institute; Professor Gene Stouder, Southwest Texas State University; Professor Bassam Matar, Glendale Community College; Professor Carlo Sapijaszko, DeVry Institute of Technology; Professor George Shaiffer, Pikes Peak Community College; Professor Val Shires, Gwinnett Technical Institute; and Professor Devinder Sud, DeVry Institute.

Hong Xiao
2001

Preface to the Second Edition

When the first edition was published in 2001, the leading-edge IC technology node was about 130 nm. Shortly after the publication of the first edition, I attended an international IC technology conference where 90 nm was the leading-edge technology node of IC manufacturing. Former Honda CEO Hiroyuki Yoshino gave a keynote speech in which he talked about ASIMO, the robot Honda introduced in 2000. At that time, ASIMO could understand some simple words and follow few verbal instructions to walk slowly and speak simple words. Mr. Yoshino envisioned that in the future, humanoids like ASIMO would be able to run, walk forward and backward, and navigate stairs. Not only would they be able to understand speech, but they could also understand the speaker's mood. They would be able to identify individuals and human emotions through facial-image recognition software. However, 90-nm technology was not sufficient to achieve these technologies, and Mr. Yoshino believed that 22-nm-technology IC chips would be needed.

A decade later, cutting-edge IC technology has reached 22 nm. An all-new ASIMO was introduced in 2011 that can run, dance, and use sign language. Whereas the older version of ASIMO is an "automatic machine" that needs an operator, the new ASIMO is an "autonomous machine," which means it can make its own decisions and actions based on environmental sensors. It has the intelligence to walk among a group of people without collision by adjusting its movement through the observation and prediction of others. It has the capability to recognize the voices of multiple people, and its image sensor is capable of facial recognition. Although the new ASIMO has made a huge improvement, it is still far from having the envisioned emotion and mood recognition capabilities; to achieve that, perhaps sub-10-nm-technology IC chips are needed.

There have been many changes in the semiconductor industry and its manufacturing technologies over the last decade. Although Intel still keeps the bulk of its IC manufacturing technology in North American fabs, the center of IC manufacturing has shifted to East Asia, in nations such as Taiwan, North and South Korea, and China. The IC manufacturing fabs in Europe, Japan, and North America are declining at an alarming rate.

The biggest challenge for IC-technology node scaling has always been patterning technology. As suggested by my predictions in the first edition, unforeseen innovations such as immersion lithography and multiple patterning

have extended the application of optical lithography and further delayed the development of next-generation lithography.

Many people helped me write this second edition. The book would not have been possible without the encouragement and support from my wife, Liu (Lucy) Huang. My elder son, Jarry Xiao, proofread several chapters. My current and former colleagues provided many useful suggestions; I would like to express my deepest appreciation to Paul MacDonald, Pierre Lefebvre, and Alan Liang.

Hong Xiao
October 2012

List of Acronyms

3MS	trimethylsilane or $(CH_3)_3SiH$
4MS	tetramethylsilane or $(CH_3)_4Si$
α-Si	amorphous silicon
AA	active area
AAPSM	alternating aperture PSM
ADC	automatic diameter control
ADI	after-development inspection
AFM	atomic force microscope
ALD	atomic layer deposition
ALU	arithmetic-logic unit
AMU	atomic mass unit
APCVD	atmospheric pressure CVD
AR	adsorption rate
ARC	antireflective coating
ASIC	application-specific integrated circuits
AttPSM	attenuated PSM
BARC	bottom antireflective coating
BEoL	back-end of the line
BL	bitline
BLC	bitline contact
BOE	buffered oxide etch
BOX	buried oxide
BPSG	borophosphosilicate glass
BSG	borosilicate glass
BST	$Ba_{0.6}Sr_{0.4}TiO_3$
BTBAS	bis-(tertiary-butylamino)silane] or $SiH_2[NH(C_4H_9)]_2$
bWL	buried wordline
C2C	cell-to-cell (inspection)
CB	contact to bit line
CBH	carborane or $C_2B_{10}H_{12}$
CD	critical dimension
CHO	cyclohexene oxide or $C_6H_{10}O$
CISC	complete instruction set computers
CMOS	complementary metal-oxide semiconductor
CMP	chemical mechanical polishing/planarization
CNT	carbon nanotube
CPU	central processing unit
CR	chemical reaction rate

CS	contact to source line
CVD	chemical vapor deposition
CZ	Czochralski (method)
D2D	die-to-die (inspection)
D2DB	die-to-database (inspection)
DEMS	diethoxymethylsilane or $C_5H_{14}Si$
DFM	design for manufacturing
DHF	diluted HF
DI	deionized
DMAH	dimethylaluminum hydride or $Al(CH_3)_2H$
DOF	depth of focus
DPP	discharge-produced plasma
DPT	double-patterning technology
DR	deposition rate
DRAM	dynamic random access memory
DSC	dichlorosilane (or dichloride silane) or SiH_2Cl_2
DSP	digital signal processing
DUV	deep ultraviolet
EBDW	electron beam direct write
EBI	electron beam inspection
EBR	edge-bead removal
ECD	electrochemical deposition
ECMP	electrochemical mechanical polishing
ECP	electrochemical plating
ECR	electron cyclotron resonance
EDA	electronic design automation
EEPROM	electric erasable programmable read-only memory
EGS	electronic-grade silicon
EMR	electromigration resistance
EOT	effective oxide thickness
EPD	electroplating deposition
EPROM	erasable programmable read-only memory
ESL	etch-stop layer
EUV	extreme ultraviolet
F/C	fluorine-to-carbon (ratio)
FEM	focus exposure matrix
FEoL	front-end of line
FET	field effect transistor
FOUP	front-opening unified pod
FPD	flat-panel display
FPGA	field-programmable gate array
FSG	fluorinated silicate glass
FTES	fluorotriethyloxysilane or $FSi(OC_2H_5)_3$

FTIR	Fourier transform infrared
FZ	floating zone
GPS	global positioning system
HDD	hard disc drive
HDP	high-density plasma
HDP-CVD	high-density plasma CVD
HEPA	high-efficiency particulate air (filter)
HKMG	high-κ and metal gate
HMDS	hexamethyldisilazane or $(CH_3)_3SiNHSi(CH_3)_3$
HOT	hybrid orientation technology
HP	half-pitch
IC	integrated chip
ICP	inductively coupled plasma
IDLH	immediate danger to life and health
IDM	integrated device manufacturer
ILD	interlayer dielectric
IMD	intermetal dielectric
IR	infrared
KGD	known good die
LAT	large angle tilt
LCD	liquid crystal display
LDD	lightly doped drain
LED	light-emitting diode
LELE or LE^2	litho-etch-litho-etch
LER	line edge roughness
LFLE	litho-freeze-litho-etch
LOCOS	local oxidation of silicon
LPC	landing pad contact
LPC	large-particle count
LPCVD	low-pressure chemical vapor deposition
LPP	landing pad poly
LPP	laser-produced plasma
LTE	low-temperature epitaxy
LWR	line width roughness
MBE	molecular beam epitaxy
MEMS	microelectromechanical systems
MEoL	mid-end of line
MERIE	magnetically enhanced RIE
MFC	mass flow controler
MFP	mean free path
MGS	metallurgical-grade silicon
MOCVD	metal organic CVD

MOS	metal-oxide semiconductor
MOSFET	metal-oxide-semiconductor field effect transistor
MRAM	magnetoresistive random access memory
MuGFET	multiple-gate field effect transistor
MW	microwave
NA	numerical aperture
NGL	next-generation lithography
NIL	nanoimprint lithography
nMOS	n-type MOS
NU	nonuniformity
NVM	nonvolatile memory
OMS	optical measurement system
OPC	optical proximity correction
OSG	organosilicate glass
OSHA	Occupational Safety and Health Administration
PBL	poly-buffered LOCOS
PC	personal computer
PCB	printed circuit board
PD	passivation dielectric
PEB	postexposure bake
PECVD	plasma-enhanced CVD
PEL	permissible exposure limit
PFC	perfluorocarbon
PIII	plasma immersion ion implantation
PLAD	plasma doping
PM	preventive maintenance
PMD	premetal dielectric
PMMA	polymethylmethacrylate
pMOS	p-type MOS
POCL	phosphorus oxychloride or $POCl_3$
PR	photoresist
PSG	phosphorous silicate (or phosphosilicate) glass
PSM	phase shift mask
PVA	poly-vinyl-alcohol
PVD	physical vapor deposition
RC	resistance $\times$ capacitance
RCA	Radio Corporation of America
RG	recessed gate
RIE	reactive ion etch
RISC	reduced instruction set computer
RP	remote plasma
RPCVD	remote plasma CVD

RTA	rapid thermal annealing
RTCVD	rapid thermal CVD
RTO	rapid thermal oxidation
RTP	rapid thermal process
SAC	self-aligned contact
SA-CVD	subatomic CVD
SAPD	spacer (self-) aligned double patterning
SA-STI	self-aligned shallow trench isolation
SC	standard cleaning
SCE	short channel effect
S/D	source/drain
SDE	S/D extension
SEG	selective epitaxial growth
SEM	scanning electron microscope
SIMOX	separation by implantation of oxygen
SIMS	secondary ion mass spectroscopy
SMIF	standard mechanical interface
SMO	source-mask optimization
SMT	stress memory technique
SN	storage node
SNC	storage node contact
SOC	system on chip
SOD	spin-on dielectric
SOG	spin-on glass
SOI	silicon-on-insulator
SPC	statistic process control
SRAM	static random access memory
SSD	solid-state disk/drive
SSOI	strained silicon-on-insulator
STI	shallow trench isolation
STM	scanning tunneling microscope
TCE	trichloethylene
TCP	transformer-coupled plasma
TCS	trichloride silane (or trichlorosilane) or $SiHCl_3$
TDEAT	tetrakis-diethylamidotitanium-titanium or $Ti[N(C_2H_5)_2]_4$
TDMAT	tetrakis-dimethylamido-titanium or $Ti[N(CH_3)_2]_4$
TEM	transmission electron microscope
TEOS	tetraethoxysilane (or tetraethylorthosilicate) or $Si(OC_2H_5)_4$
TMA	trimethylaluminum or $Al(CH)_3$
TMAH	tetramethyl ammonium hydroxide or $(CH_3)_4NOH$

TMB	trimethylborate or $PO(OCH_3)_3$
TMP	trimethylphosphite or $P(OCH_3)_3$
TSV	through-silica via
TW	thermal wave
UHV	ultrahigh vacuum
UHV-CVD	ultrahigh-vacuum CVD
ULK	ultralow-κ
ULSI	ultralarge-scale integration
USG	undoped silicate glass
USJ	ultrashallow junction
UV	ultraviolet
VLSI	very large-scale integration
WCVD	tungsten CVD
WERR	wet etch rate ratio
WID	within die
WIW	within wafer
WL	wordline
WTW	wafer to wafer
XRR	x-ray reflectometry