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Control of IC Patterning Variance Part 1: Metrology, Process Monitoring, and Control of Critical Dimension

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The field of CD-related metrology for process control went through a decade of rapid change. New metrology applications for direct estimation, monitoring, and control of key process parameters, such as effective exposure dose and focus in lithography, have emerged. They have enabled optical microlithography extensions to the diffraction limit for the smallest resolvable pitch and even beyond (with pattern multiplication). The arguments for direct metrology of dose and focus for better CD control are now over. What used to be the "off the roadmap metrology" is now a part of ITRS.

The following are published in this special section:

Bertrand Le-Gratiet et al. discuss the sources of CD variation and present applications of dose and focus monitors to CD control for advanced node production. One of the most profound aspects of their work is the degree of dose and focus metrology integration: the tools' on-board and on-product process monitors are used to map both across-field and across-wafer dose and focus variations, enabling their compensation during scan. This change is as revolutionary as using interferometry for the control of mechanical stages.

The field of dimensional metrology itself is also changing. François Weisbuch and Kenneth Jantzen discuss a design-based metrology where scanning electron microscope (SEM) contours are used for measurements of not only critical dimensions of a few linear (1-D) features but also of feature edge placement anywhere along any feature in the context of optical proximity correction (OPC) model building and validation.

Eitan N. Shauly et al. present a generally applicable methodology of calibrating such CD-SEM contour-based measurements in device layouts in SPICE simulation, using extracted device parameters as the inputs, to produce the effective physical dimensions for the shapes measured. This way, both single-layer design rules (DRs) and two-layer DRs (area of overlap or edge-to-edge overlay) are measured—despite a possible partial obscuration of the reference layer—and also calibrated to device performance. This is possibly the most effective way to monitor and validate DR compliance in production.

Deborah A. Ryan et al. take such a capability to a completely new level: inspection. Their paper covers the applications of e-beam inspection for the detection of hot spots, such as in OPC model validation and optimization or post-tapeout validation, and for early detection of systematic patterning problems and marginalities in advanced SOI FinFET technology front end and dual Damascene metallization back end.

Ahmad Faridian et al. present the model-based analysis of phase-sensitive structured illumination for the application of detecting and gauging the dimensions of nanosized asymmetries in silicon trenches with novel scanning optical microscopy and image analysis.

Dhairya J. Dixit et al., on the other hand, already are looking at directed self-assembly (DSA) and potential applications of Mueller-matrix-based scatterometry in CD metrology and characterization of DSA processing effects affecting pattern sidewall and regularity.

We hope you will find these papers of relevance and interest to your work.

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