Digital pattern generator: an electron-optical MEMS for massively parallel reflective electron beam lithography

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1 Introduction

Optical lithography has been the mainstay in sustaining Moore’s law, taking us to 28 nm half pitch and beyond. To cope with feature-size shrink to well below the wavelength of 193 nm, new refinements, such as optical proximity correction (OPC) and multiple patterning, have been incorporated, but at a greatly increased cost. Extreme ultraviolet lithography (EUVL) has been touted as a successor to optical lithography, but delays in its development mean its adoption will occur at a feature size smaller than its wavelength of 13.5 nm; therefore legacy complexities from optical lithography such as OPC and multiple patterning will likely have to be retained, and at the same time new challenges such as source power, mask defects, and resist sensitivity will have to be overcome.

Traditional e-beam lithography suffers from low throughput and was generally deemed not suitable for high-volume manufacturing (HVM). However, advances in micro electromechanical systems (MEMS) technology in the last decade have enabled the pixilation of a high-current e-beam, enabling massively parallel e-beam writing. E-beam lithography thus has the potential to become competitive with optical or EUV lithography, especially in foundry applications in which the mask cost may not be efficiently amortized.

KLA-Tencor is developing reflective electron beam lithography (REBL) technology to enable maskless lithography for HVM of semiconductors at 14 nm half pitch and beyond. Each e-beam column consists of illuminating and imaging optics. An off-axis illuminating beam is merged into the optical axis of the e-beam column through a Wien filter and illuminates an active area of 0.4 mm × 6.6 mm of the digital pattern generator (DPG), which is an electron-optical MEMS consisting of a 248 × 4096 array of 1.6 μm pitch lenslets. Through the selective application of a positive or negative bias on the bottom of each lenslet, the electron beamlet is absorbed or reflected, respectively. The pixilated overall image of the DPG is then demagnified 100× or greater onto the wafer. To further increase throughput and reduce overall system risk, REBL is considering having multiple columns and replacing a previously planned rotary stage concept with a dual action, linear stage technology (Fig. 1). With sufficient multiple columns, this architecture can potentially produce commercially practical wafer throughputs for HVM of semiconductors.

The focus of this paper is on the DPG, which is the technology that enables massively parallel printing with significantly increased throughput compared to single raster beam lithography. We will discuss four specific aspects of the DPG technology: the design of the underlying CMOS circuit that...
drives the lenslets, the modeling of the lenslet structure that led to our final lenslet design, the fabrication of the DPG, and the mitigation of charging on the DPG. Finally, we present test results.

2 Underlying CMOS Design

REBL is unique due to its use of reflective electron-optics to pattern an electron beam. This is done by selective reflection of a low-energy “flood” illumination beam from an array of switchable electron mirrors. The spatially patterned beam is then accelerated, demagnified, and focused onto the resist-coated substrate being patterned. Each electron mirror is operated in binary mode, either ON or OFF. Initially, it was thought that simple electrodes would suffice for the reflectors: if given a small positive potential, an electrode would absorb the impinging beamlet, turning that mirror off; or if given a small negative potential, the electrode would reflect, turning that mirror on. Experiment and simulation quickly convinced us that in fact each electron mirror would require, in addition to the switched mirror electrode, a tiny electron-optical assembly, with several electrodes stacked above the mirror electrode and driven at fixed potentials, whose function is to gather, steer, and focus the beamlet. The assembly of mirror-electrode drive circuits and miniature electron-lens assemblies is called the DPG. The construction of the DPG therefore involves both CMOS electronics and an integrated MEMS assembly.

To synthesize gray tones of exposure, REBL uses a technique called time-domain integration (TDI), which works as follows. The DPG is constructed as a two-dimensional (2-D) array of electron mirrors. At exposure time, the wafer being printed is moved smoothly across the field of the projection (demagnifying) electron-optics. As any given spot on the wafer passes under the image of the DPG, it is sequentially exposed to the reflected electrons from a specific row of DPG mirrors (Fig. 1). As the wafer moves, the pattern of ON mirrors on the DPG moves in synchronization so that the electrons reflected from successive mirrors in each row fall onto the same spot on the wafer for the entire time that the spot in question is within the area covered by the DPG image. By controlling which mirrors in each row are ON, the DPG’s control logic ensures that each spot on the wafer receives an energy dose proportional to the gray tone designated for it.

Each electron mirror is binary, i.e., ON or OFF at any instant. The mirror array is partitioned into bit-blocks to produce a grayscale 0 to 31; for example, one can use a block $N$-mirrors wide to provide the dose corresponding to the least significant bit, or bit 0, of the desired gray level being ON, another bit-block $2N$-mirrors wide to provide the dose corresponding to bit 1 of the desired gray level being ON, a block $4N$-mirrors wide to provide the dose corresponding to bit 2 of the gray level being ON, etc., up to the largest bit-block $16N$-mirrors wide to provide the dose corresponding to the most significant bit of the gray level (bit 4 in this case). Since no mirrors are required to represent a dose of 0, the total width of the mirror array is $31N$ mirrors. We chose $N = 8$, making our mirror array 248-mirrors wide. This choice is a practical compromise between the desire to compensate spatial nonuniformity of lenslet efficiency and illumination, which favor a large $N$, and the need to minimize an uncorrectable blur in the direction of the stage motion, which favors a small $N$. To make the bit-weights add up correctly, each pixel of incoming gray data is broken up into its constituent bits, and the various bits are delayed appropriately so that each controls in succession the mirrors of its corresponding bit-blocks, and the apparent movement of the projected image matches the movement of the wafer. The bits are delayed again after their traverse across (a portion of) the mirror array; this permits reassembly of the gray data in order to verify that the data were printed correctly.

The initial concept of REBL had some additional constraints on the design of the mirror array and its CMOS mirror-switching circuits. We began with a plan to print IC patterns in a continuous, spiral swath across multiple wafers on a rotating stage platter. The small differences in radius from the axis of rotation to the pixel-rows would have resulted in a gray-tone-dependent blur; to counteract this, the bit-blocks were each divided in two (except the bit 0 block), and the two halves were arrayed symmetrically about the mid-line of the mirror array. Figure 2 illustrates the division of the array into bit-blocks. Since then, we have shifted to a linear platform, but we retained the symmetric layout on the DPG to avoid a major redesign.

The individual mirror driver circuit needs to be small so that it will fit under the lenslets and not require excessive demagnification of the projection electron-optics: high demagnification would cause either large spherical aberration or inefficient use of the illumination current. The
mirror-driver circuit needs to switch the mirror electrode through a relatively large potential difference, which we estimated at up to \(2.5\ \text{V}\), in order to ensure adequate contrast. The circuit was to be fabricated in 65 nm low-power CMOS, for which core transistor \(V_{dd}\) is nominally 1.25 V. The use of \(I/O\) transistors to obtain higher voltage switching was considered but deemed unfeasible because of their large size. We commissioned a full-custom circuit design in order to strike a good compromise among these competing constraints. A 10-transistor unit-cell circuit that could be built in a 1.6 \(\mu\)m square area was designed. Various stratagems, including long channels and level-shifters, were employed to make the circuit tolerant to higher-than-normal \(V_{dd}\). The delay lines, which were used on the input side to align the contributions of the various bit-blocks, in the middle to bridge between the two parts of bit-blocks 1 through 4, and on the output side to reconstruct the pixel data, are ring-buffers constructed from static RAM arrays—they do not have to tolerate the relatively high \(V_{dd}\). After the CMOS circuit was fabricated, testing determined that it is sufficiently robust to operate at \(V_{dd} = 2.5\ \text{V}\).

With the mirror pixel pitch fixed at 1.6 \(\mu\)m, the length of the mirror array was determined by the limitation of the electron-optics. Analysis by ray-tracing indicated that field distortion limits the array to \(\sim 6\ \text{mm}\) long. Consequently, the array length was chosen to be 4096 rows, which corresponded to a length of 6.6 mm.

The overall chip design included input circuits for the incoming data and output circuits for data verification. In order to keep the chip reasonably simple, we decided to limit the amount of data that the first CMOS chip would be expected to handle: we drive 256 pixel-rows \(\times 5\) bits of input data, and fan that out to the 4096 pixel-rows. The input data are time-domain multiplexed so that 256 wires each accept 5 bits, with the help of a 5-phase clock. Simulation showed that the mirror array could operate at up to 100 M lines per second. Though the individual mirror-cell can operate in excess of 200 MHz, the performance of the array is limited by factors such as clock skews. Our first CMOS chips showed pixel-row yield in excess of 99.5%, which was acceptable at the early stage of technology development. The target pixel-row yield for production remains at 100%, i.e., perfect devices.

3 First-Generation DPG with Planar Design

A DPG design prior to the one reported here used a planar, 2-D structure, shown in Fig. 4. The individual pixel consisted

![Fig. 3](https://example.com/fig3.png)

**Fig. 3** Symmetrized bit-block scheme, for 4-bit gray scale and “redundancy” \(N = 1\).

![Fig. 4](https://example.com/fig4.png)

**Fig. 4** Scanning electron micrograph of planar DPG (first generation) without any lenslets.
simply of a 0.5-μm-thick square pad of TiN connected directly to the CMOS output for the pixel below. A bias of 0 or 2.5 V was applied to put the pixel in a dark or bright state, respectively. However, initial testing revealed that the feature size did not scale with the number of ON mirrors. It became evident to us that we needed to improve our electron-optical design.

4 Why Two-Dimensional Mirrors Were Insufficient: Lack of Linearity

To print an image, REBL modulates the exposure intensity at each resist exposure element (pixel) of the printed area; the net modulation is the superposition of a sequence of aerial images formed by electron reflection from its CMOS-driven DPG. A principal goal of the exposure modulation is to place images formed by electron reflection from its CMOS-driven DPG. A principal goal of the exposure modulation is to place images formed by electron reflection from its CMOS-driven DPG. A principal goal of the exposure modulation is to place images formed by electron reflection from its CMOS-driven DPG. A principal goal of the exposure modulation is to place images formed by electron reflection from its CMOS-driven DPG. A principal goal of the exposure modulation is to place images formed by electron reflection from its CMOS-driven DPG. A principal goal of the exposure modulation is to place images formed by electron reflection from its CMOS-driven DPG. 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A principal goal of the exposure modulation is to place images formed by electron reflection from its CMOS-driven DPG. A principal goal of the exposure modulation is to place 4.1 Achieving Linearity Through the Use of Lenslets

The linearity requirement led to the need for a 3-D electrostatic lenslet for each pixel in order to isolate the fields of different pixels from one another. The resulting lensing action of this 3-D lenslet must emulate a switchable micro-mirror. Figure 6(a) shows two equal converging lenses sharing the same focal plane; this system forms a telecentric doublet with two conjugates points P and P’. If P is...
In order to provide enough focusing action, its bias \((VM)\) must be a few times \(VU\) (\(VM \approx 30\ V\)). Finally, the bottom electrode is the reflecting electrode or electrostatic mirror section. Its bias \(VB\) must be adjusted so that it will reflect as much beam as possible in the ON state, and as little beam as possible in the OFF state. The difference between the ON and OFF potentials, \(\Delta V_0\), must not exceed the range than can be supplied by the CMOS mirror-drive circuit, which is 2.5 V. The largest bias difference between adjacent electrodes is approximately \(VM - VU \approx 20\ V\); this requires an interlayer dielectric of about 1 \(\mu\)m to avoid electrical leakage or breakdown.

Another important parameter is lenslet efficiency \((\eta)\), which is the ratio between the illumination current collected by the lenslet and the reflected current (beamlet) from that lenslet, which is collected by the imaging optics; this ratio is also equal to the ratio between the angles \(\alpha'\) and \(\alpha\), where \(\alpha\) is the NA of the system [Fig. 6(c)] and \(\alpha'\) is the NA of a beamlet. The NA of the REBL projection optics is 12 mRad. In other words the lenslet, in order to be efficient, must be telecentric at least within an angle equal to the NA of the system. Furthermore, when the bottom electrode is in the OFF state, the reflected beamlet current must be as small as possible; the contrast measures this ability as the ratio between the beamlet current \((I_{ON})\) and the beamlet current obtained with a biased bottom electrode \((I_{OFF})\).

### 4.2 Pentode Optimization, Contrast, and Yield

The following optimization method was employed to find the best bias settings for the lenslet design of Fig. 4. The top electrode voltage \(VT\) and the switching voltage \(\Delta V\) were kept constant \((VT = VT_0 = 5\ V, \Delta V = \Delta V_0 = 2\ V)\). The minimization space was therefore a four-dimensional (4-D) space \((VU, VM, VL, VB)\) and the figure of merit to be minimized was \(\chi = 1 - \eta \times (I_{ON} - I_{OFF})/(I_{ON} + I_{OFF})\), in which \(I_{ON}\) was given by a point in the optimization space and \(I_{OFF}\) was given by the same point where \(VB\) has been incremented to \(VB + \Delta V_0\). With this figure of merit the method will converge to a set of four voltages when \(\eta \approx 1\) and \(I_{ON} \gg I_{OFF}\). The optimization method used in this design is the differential evolution method applied to the four-dimensional function \(\chi = \chi(VU, VM, VL, VB|VT_0, \Delta V_0)\). This function was calculated numerically by
the unipotential method and by tracing a fixed bundle of rays with a defined energy spread. Figure 8 shows the optimization result. The biases applied to the electrodes must be accurate to within \( \pm 100 \text{ mV} \). The ray tracing in Fig. 8 was performed with the optimized voltages and under the assumption that an image of the source was formed at the point \( P \) (thus IP at the entrance of the lenslet is a plane conjugate to the source). Ray bundles corresponding to \( I_{\text{ON}} \) and \( I_{\text{OFF}} \) are shown in Fig. 8. The ray tracing shows that a back focal plane (\( F \)) is formed at the turn-around point; it also shows that the mirror, or the bottom electrode, has a positive focusing action given by the parabolic form of its equipotential lines. Figures 8 and 9 show that this focusing creates an image plane \( P' \) inside the lenslet. Since the optimization method seeks to establish a telecentric condition, a negative lensing term \( D_1 \) must appear to compensate for it. As a result, the final image of the source that is formed by the lenslet is virtual (point \( V \)) and it is telecentric within the NA of the system; thus the paraxial rays for both \( P \) and \( V \) have the same angles with respect to the axis. Figure 9 shows another schematic of the optimization result, in which the reflected rays have been unfolded for clarity. Note that the diverging component \( D_1 \) affects mostly the magnification between the image in \( P' \) and in \( V \). Therefore its effect on the paraxial illumination rays has been omitted for simplicity. When adding a switching voltage (\( \Delta V_0 = 2.5 \text{ V} \)) to the bottom electrode voltage, the virtual image will have no paraxial rays with angles smaller than the NA of the system and, therefore, will not appear at the wafer. Figure 10 shows a comparison between an ON and an OFF beamlet. The OFF beamlet is moved out of the aperture. Figure 11 shows how this switching principle is integrated in the system. It is important to point out that the switching mechanism discussed above does not require the whole beam to be absorbed by the bottom electrode. This helps to maintain a high contrast in the presence of an energy spread larger than the CMOS switching voltage.

The lenslet structure previously discussed needs to maintain not only linearity but also high efficiency and high

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**Fig. 9** Unfolded paraxial rays for optimized lenslet.

**Fig. 10** Switching mechanism produced by the optimization method.

**Fig. 11** Integration of the switching mechanism in the system.
contrast when the illumination energy spread becomes larger than the CMOS switching voltage. This requirement comes from the high beam current necessary for an acceptable throughput. At the required high beam currents, the energy spread can reach 3 eV FWHM because of stochastic interactions between electrons. Figure 12 shows the yield, which is the product between the lenslet efficiency and the pixel fill factor, and contrast as a function of the illumination energy spread. (The pixel fill factor is the ratio between the area of the lenslet physical aperture, which is about 1.4 μm in diameter, and the area of the pixel, which is 1.6 μm in pitch; so the pixel fill factor is 0.6.) The settings of the electrodes are the same as those in Fig. 7. As can be seen, the contrast reaches 100% for an electron energy spread of 2 eV FWHM. This gave us confidence in finalizing the lenslet design to the pentode.

5 Fabrication of the Pentode Lenslet Array (Gen-2 DPG) and Its Integration with the CMOS Circuit

The pentode lenslet structures were fabricated at the Imec 300 mm fab in Leuven, Belgium. The development was divided into four phases. In phase 1, the focus was on manufacturing the lenslet pentode structures, which were standalone, not connected, and done on blank 300 mm wafers. In phase 2, electrical connectivity was added, such that the optical performance could be evaluated in a static mode and with control of the lenses by the row only. In phase 3, the processing was adapted to fabricate the devices on top of CMOS with the bottom of each lenslet connected to the CMOS circuit. The CMOS wafers were fabricated by Taiwan Semiconductor Manufacturing Company (TSMC) using 65 nm LP technology with 9 metal layers. This allowed for the individual control of the lenslets. Some design choices in phase 3 proved not sufficiently robust for wirebonding. Therefore, a fourth phase was added to improve the robustness. This improved design showed good yield, performance, and stability.

5.1 Fabrication of Lenslet Pentode Structure

The lenslets consist of a densely packed 248 × 4096 array of 4-μm-deep cylindrical holes on a 1.6-μm pitch through an alternating stack of four conductive TiN layers and four insulating SiO2 layers (Fig. 14). Top and bottom electrodes are 300 nm thick physical vapor deposition (PVD) TiN layers. The intermediate electrodes consist of 60 nm PVD TiN. Between the electrode layers are the SiO2 dielectric layers deposited by plasma-enhanced chemical vapor deposition, with thicknesses between 750 and 900 nm. The top spacing between the holes (edge-to-edge) was targeted at 200 nm. This is to maximize the contrast while maintaining mechanical integrity of the lenslet structures.

The large etch depth of 4 μm and the resolution of 200 nm spacing between the holes with a 10 nm hole uniformity across the array required an advanced dual hard mask-based patterning scheme in combination with 248 nm wavelength lithography. A thin resist was chosen to pattern a thick hard mask stack that was then used as a masking layer to transfer the pattern of the holes in the 300 nm TiN and 3.6 μm oxide stack. The results of the initial etch developments are shown in Fig. 13 (bottom). Note that the thin TiN layers at intermediate electrode levels had already been opened with a diameter for the higher electrode always 40 nm larger than the electrode below. This funnel shape provided an overlay...
margin of 20 nm from one electrode level to the next. The margin ensures that each electrode is fully exposed after the final etch.

5.2 Static Lenslet Device

In this phase, electrical connections were added to the standalone lenslet structures such that the 4096 lenslets on every row were electrically joined and connected to one bond pad per row. Many processing steps and additional exposure masks were needed to fabricate and pattern the electrical connections. Three via layers were added below the bottom electrode to connect the different electrode layers. The lower, middle, and upper electrodes were patterned to form segments with connections to bond pads. An aluminum layer was added in between upper and top electrodes to form bonding pads, and the top TiN layer was patterned to separate the pads. The top layer was opened in the bond pad region to reach the aluminum bonding layer. Figure 14 shows a schematic cross-section of the lenslet devices with the connections to bond pads.

The bottom electrode was patterned with lines (1.4 μm wide and 200 nm spacing) such that the 4096 lenslets on every row were electrically joined and connected to one bond pad per row. The vertical interconnects between the different electrodes (bottom, lower, middle, and upper) were formed by arrays of vias in the pad area. To minimize process complexity, the via levels were not metalized separately; instead, the TiN of the electrode layers was used to provide electrical connection between the different levels. The resistance of a single via was 1 kΩ. By combining the vias in arrays, the connections between different levels could be kept below 10 Ω.

Unlike conventional bonding pads that are manufactured on top of the device, our Al bonding pads were formed between the upper and the top electrode layer. This was done to avoid pad processing after the lenslet holes have been opened.

5.3 Integration of Lenslet Devices onto the CMOS DPG Wafer

In the third phase, the process was augmented to integrate the lenslets on top of a CMOS wafer with a full nine-level interconnect stack. This would enable the full control of individual lenslets. A via opening through the passivation layer on top of metal 9 was added to connect the top metal level to the first electrode level. The bottom electrode layout was changed from a line pattern, which bunched the lenslets into rows, to a circular plate, which allowed the lenslets to be addressed individually. The probing pads were redesigned to provide a low resistive connection from probing pad to top metal level of the CMOS wafer. The changes are schematically shown in Fig. 15.

The vias between metal 9 and the bottom electrodes were made by etching 900-nm-diameter holes in a 150-nm-thick CMOS passivation stack. An individual via under each lenslet allows control of every lenslet individually. The bottom TiN layer was deposited over the via holes and patterned with 1.4 μm circles for each lenslet. The via in the center of each electrode circle creates the donut-like shapes in Fig. 16.

The connection from bonding pads to the CMOS at the top (metal 9) level of the DPG CMOS chip is required to have a...
resistance of <0.2 Ω. This cannot be achieved with the TiN-filled via arrays that were used for the static chip design. The TiN layers have a resistivity of 150 μΩ-cm, which is too high to meet the 0.2 Ω requirement. For the bond pad to the bottom electrode, placing the Al bonding layer directly on top of it (instead of near the top) would bypass the TiN layers and greatly lower the resistance (Fig. 15, left). An oxide patterning step is required to expose the aluminum layer. For the pads that connect to one of the top four electrodes (Fig. 15, right), arrays of vias are still used to connect the layers. These electrodes operate on static voltage and carry very small currents; therefore the resistance of these connections is not critical, and the solution with TiN via arrays developed in phase 2 can still be applied. Figure 17 shows some images of the completed device.

After the devices were built in the above manner, electrical shorts were found during testing between the bottom TiN plate and the top Cu layer. Many of these defects appeared after postprocess wire-bonding, indicating that wire-bonding was responsible for creating shorts between the pad and the underlying metal. We concluded that the CMOS design was not ideal for the additional lenslet processing because of the presence of metal lines directly underneath the pads. This was aggravated by the presence of a thin insulating layer of 150 nm separating the bond pads from metal lines in the initial design; this thin insulating layer proved too easy to puncture during wire-bonding. In the next section, we show how this issue was addressed.

5.4 Modified Process for Lenslet Devices on CMOS DPG Wafers

Two modifications (Fig. 18) were implemented to help prevent shorting to the metal lines in the CMOS. The first was doubling the Al pad thickness. With this modification, the chips passed electrical test and were demonstrated operational for the first time. However, the performance and resolution of this first functional device were still limited. Performance was further improved by adding a dielectric layer between the passivation and the first electrode and by using a Cu filling of the via to make the interconnect to the underlying metal. The thicker dielectric layer further protects the underlying metal lines. The Cu filling enhances contact with the bottom electrode. Figure 22 shows the stack structure before and after these process modifications.

6 Overcoming Electrostatic Charging

Initial electron-optical testing of the DPG lenslets fabricated by Imec revealed that there was considerable electrostatic charging that interfered with the proper operation of the lenslets. The kinetic energies of the electrons in the lenslets are low; thus they can easily become embedded in the dielectric oxide. Our mitigation strategy was to apply a conductive coating onto the lenslets to drain the charge. This coating
must have a resistance that is low enough to drain the charge, but not so low that it short-circuits the electrodes in the lenslets. Also, because a uniform coating needed to be applied to all surfaces of the high-aspect-ratio lenslets, the film must be deposited isotropically.

Initially, we employed a coating composed of a homogeneous mixture of two binary oxides, such as Ta$_2$O$_5$ and Nb$_2$O$_5$, deposited by atomic layer deposition (ALD) to achieve an isotropic coating. The resistivity of the coating can be customized by adjusting the ratio of the two species. However, we found during testing that the film would undergo a slow breakdown and its resistivity would degrade in a matter of weeks under the high electrical field between the electrodes (up to 25 MV/m). An alternative coating composed of nanoclusters of a conductive oxide (MoO$_{3-x}$) embedded in a matrix of Al$_2$O$_3$ was employed in its place. This coating, which was also deposited by ALD, had been developed at Argonne National Laboratory for the purpose of charge draining in microchannel plates. The detailed mechanism of conduction has been described in detail elsewhere.

In short, the MoO$_{3-x}$ nanoclusters act as dopants to the Al$_2$O$_3$ matrix, while the amorphous Al$_2$O$_3$, which has very high mechanical and dielectric strengths, served to protect the MoO$_{3-x}$ from breakdown. The resistivity of material can be customized by adjusting the concentration of MoO$_{3-x}$. Cross-section transmission electron micrographs of the film are shown in Fig. 20. Application of this coating to the DPG resulted in its stable operation for three months.

7 Imaging and Print Results

Figure 21 shows images produced by the DPG with the pentode lenslets and the MoO$_{3-x}$/Al$_2$O$_3$ charge-drain coating. With the working DPG, we proceeded to perform the first functional test of all aspects of the TDI printing system: CMOS DPG, rendering, data clocking, and stage metrology. Figure 22 shows print results produced by the patterns on a chemically amplified resist and poly(methyl methacrylate).

8 Summary

The DPG is a complex electron-optical MEMS that pixelates the electron beam in the REBL e-beam column. It potentially enables massively parallel printing, which could make REBL competitive with lithography for semiconductor manufacturing. In this paper, we described the development of the REBL DPG, from the CMOS architecture, through the...
pentode design, to the fabrication of the MEMS device. The imaging and printing results validated our pentode lenslet concept and the fabrication process. The successful development of the DPG has enabled us to proceed with full-scale fine-tuning of the e-beam column and process development.

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Biographies and photographs of the authors are not available.