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Alexander Starikov

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Control of Integrated Circuit Patterning Variance, Part 4: Placement and Critical Dimension, Edge to Edge Overlay

Alexander Starikov
I&I Consulting
Palo Alto, California, United States

This special section builds on high interest in Control of IC Patterning Variance Part 2: Image Placement, Device Overlay and Critical Dimension and on increased industry attention to "anything overlay" at, and around, SPIE Advanced Lithography.

Although SEMI Standard P18-92 defines "good fields" as limited by overlay, it is now widely accepted that overlay alone does not limit the device yield and cell scaling. The limitation is due to edge-to-edge overlay, the distance between an edge of a pattern in one layer and an edge of a pattern in another layer. It contains overlay and per-side deviations of the layer linewidths. This distance being the limiting factor has been known for decades.[1–3] In the days when 98% of it was due to overlay, it was used to designate overlay as the 256 Mb technology roadblock. After three decades of overlay improvements, long after 256 Mb went to production, that distance is no longer as dominated by overlay. Problem is, our industry not having established a capability to directly measure that distance, its control lags the need and that causes industrywide losses. By now, the industry demands this issue be fixed. Not helping to close the long-existing technology gap, that distance was recently named "edge placement error" (EPE), as if something new was discovered, clashing with EPE as the foundation of model-based OPC.[4] Absent industry consensus on what to measure, even what to call it, hampers the dialog on a common solution.

This special section leads the way to direct in-device metrology the industry needs, enabling superior control of pattern placement, critical dimension, and edge-to-edge overlay, or whatever its name.

The first paper, by Gabor and Felix, presents a general framework for overlay control in multi-exposure patterning where overlay and two layers' conductor lines form the dielectric of circuit wiring. Here, the descriptive term "space error" is used to refer to the combined CD and overlay error in spaces between features. This paper contains ample explanation of what to measure and to control, definitions and terminology, design rules and yield, metrology data analysis, FAB process assumptions and operations practices to maximize the "good die out." Whether a reader is new to the subject or about to implement overlay APC in a FAB, this is the place to start.

Weisbuch et al. roll out their latest in SEM contour based in-device metrology of registration and overlay and, ultimately, direct metrology of edge-to-edge overlay (termed $EPE_{interlayer}$ here) and overlap area (two design rules responsible for overlay-limited yield). To enable two-layer metrology with a partially obscured pattern as the reference they start by SEM imaging of the first layer patterned, post-etch, then aligning to it the SEM image of the second patterned layer, also post-etch, using select unobscured first layer patterns as SEM image alignment targets. Abundant metrology of device overlay, edge-to-edge overlay, and overlap area is then produced for all patterns within SEM field of view, starting with design intent in GDS and in pattern contours, physical definitions of edge, linewidth (CD), centerline (CL), overlay (OL) and $EPE_{interlayer}$, detecting edge coordinates in SEM images, followed by contour extraction and data analyses while also accounting for target- and instrument-related measurement variations.

Bizen et al. report results from a mostly modeling based study of SEM imaging to optimally detect the pattern edge at the bottom of high aspect ratio structures. Not only does this help to improve the CD metrology of HAR structures, accurately detecting the bottom edge with CD-SEM may help to overcome the inaccuracy of conventional optical metrology on targets with sidewall asymmetry, such as due to asymmetric etch process on wafer edges.

Ohashi et al. describe an inspection application with effective detection of contact opens, i.e., of functional device failures, using SEM voltage contrast. Estimation of parasitic resistance and capacitance is enabled by considering the dynamics of e-beam interaction with the device structure and comparison of experimental VC vs. VC response from a newly developed dynamic changing model.

This special section culminates with a technology review, by Inoue and Hasumi, of SEM-based overlay metrology. With SEM-based overlay metrology often bootstrapped using whatever means available and with little consideration of precision and accuracy, it is already used as a reference metrology and even for calibrating conventional optical overlay metrology in production, these authors describe this urgently needed technology in-full and in-depth for all applications: on overlay metrology structures, on device-like metrology structures, and directly on devices, for layer pairs where topography edges are readily detected by (low voltage) production CD-SEM and those that must rely on the materials contrast and high voltage, even on dynamic voltage contrast. This paper presents the state of the art in SEM based overlay metrology and shares a wealth of diverse SEM technology and SEM metrology applications know-how. Not only do you find accounts of most cases where SEM based (centerline) overlay and edge-to-edge overlay measurement can be made, but also the key technical details involved in making those measurements, performance data, analyses of metrology errors, even paths for improving SEM overlay metrology precision, accuracy, and throughput.

This special section uses rigorous definition of edge-to-edge overlay, or whatever that width is called, and demonstrates effective means to directly measure it in devices, establishing *de facto* standards, metrology capability and process control for more "good die out" and continued device cell scaling.

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