Site-specific metrology, inspection, and failure analysis of three-dimensional interconnects using focused ion beam technology

Frank Altmann
Richard J. Young

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Frank Altmann
Fraunhofer Institute for Mechanics of Materials
  Halle
Center for Applied Microstructure Diagnostics
Walter-Hülse-Straße 1, 06120 Halle, Germany

Richard J. Young
FEI Company
5350 NE Dawson Creek Drive Hillsboro, Oregon
  97124
E-mail: richard.young@fei.com

Abstract. Today three-dimensional system-in-package integration together with advanced interconnect technologies based on through silicon vias, through encapsulant vias, and microbumps are considered some of the most promising enabling technologies for "More than Moore" solutions. These technologies involve vertical die stacking or chip embedding with high-density interconnects and are based on combinations of process steps that come from formerly strictly separated technology areas. Thus, there is an increasing need to understand a large number of different interface properties, to control and optimize processes, and to avoid defect formation that could affect reliability. This complexity, in terms of design, new materials, and material combinations, also requires the development of new failure analysis tools to support these developments. The application potential of a new fast plasma focused ion beam (FIB) system for metrology and failure analysis is demonstrated in several selected case studies. The higher material removal rate of this system improves the range of application fields and/or the analysis throughput. This makes the plasma-FIB a very attractive tool for the analysis of relatively large interconnect structures without any need for mechanical preparation steps. © The Authors. Published by SPIE under a Creative Commons Attribution 3.0 Unported License. Distribution or reproduction of this work in whole or in part requires full attribution of the original publication, including its DOI. [DOI: 10.1117/1.JMM.13.1.011202]

1 Introduction

Today three-dimensional (3-D) system-in-package integration together with advanced interconnect technologies based on through silicon vias (TSV), through encapsulant vias (TEV), and microbumps are considered some of the most promising enabling technologies for "More than Moore" solutions. In particular, 3-D integration can provide significant progress in semiconductor device development regarding increased system functionality, performance, and integration density. These technologies involve vertical die stacking or chip embedding with high-density interconnects and are based on combinations of process steps that come from formerly strictly separated technology areas. Thus, there is an increasing need to understand a large number of different interface properties between different interconnects and with any encapsulation or lamination materials, to control and optimize process steps and layer thicknesses, and to avoid any defect formation that potentially could affect the component's reliability. This complexity in terms of design, new materials, and material combinations also requires the development of new system-adequate failure analysis tools capable of providing information on adhesion mechanisms, interdiffusion, and phase formation processes, or on electrical short, crack, and void formation issues.

Therefore, there is a strong demand for metrology, physical characterization, and failure analysis of a wide range of 3-D interconnect technologies and relevant processes, and also for preparation and analysis techniques that allow access to buried structures providing physical information at the nanometer scale within a large field of view. While focused ion beams (FIBs) have been used very successfully for the sample preparation that is required for advanced CMOS device analysis,[1] these systems are less suited for package-level sample preparation because of the relatively low milling rates ($\sim 10^3 \ \mu m^3 / min$), which make the removal of large volumes impractical. Recently, a new FIB technology has been developed that offers much higher material removal rates, thanks to the use of an inductively coupled plasma (ICP) xenon ion source that can deliver 20 to 50 times higher beam currents than the classical gallium liquid metal ion source (Ga-LMIS).[2–5]

Within this paper, the application potential of a new fast plasma FIB system for metrology and failure analysis is demonstrated in several selected case studies. Depending on the material under investigation, both the higher current and the higher sputter efficiency of the Xe significantly improve the range of application fields and/or the analysis throughput. This makes the plasma FIB a very attractive tool for the analysis of relatively large interconnect structures without any need of mechanical preparation steps.

2 FIB Technology

In the last 20 years, physical failure analysis, metrology, and inspection at the gate and interconnect level has come to rely on FIB to provide site-specific information about the device structure, layer thicknesses, material compositions, and defect locations and mechanisms. This is due to

FIB's ability to create highly site-specific cross-sections and transmission electron microscope (TEM) samples, and to perform gate-level circuit rewire and debug. With sectioning, the FIB can make localized openings through widely differing material types, enabling analysis on areas that would not be possible by mechanical polishing due to both the localization required (e.g., sub-15-nm-thick TEM sample must be located to within a few nanometers of the correct location), and due to sample preparation challenges, such as material smearing/tearing due to hardness differences. The localized nature of the milling also means that multiple sections (in different orientations, if needed) can be achieved even in close proximity to each other and that the rest of the device can remain intact for other analyses.

FIB systems have historically used a Ga-LMIS, providing a typical beam current range from 1 pA to tens of nA. This corresponds to a maximum material removal rate by sputtering of $\sim 10^3$ μm^3/ min for silicon at 60 nA of beam current, which enables volumes of a few tens of μm on a side (e.g., for transistor, cross-section, or TEM sample) to be removed in a reasonable time. However, many 3-D interconnect samples require much larger volume material removal than is the case with traditional FIB applications (e.g., milled volumes in the order of $100 \times 100 \times 100 = 10^6$ μm^3 and larger), so they are generally seen as being prohibitively time consuming for the standard FIB approach. This has therefore led to the development and introduction of new FIBs with much higher overall milling rates, based on the ICP source. Using ICP source technology with Xe ions enables the maximum useful beam current (and hence milling rate) to be increased by more than 20 to 50 times to >1 μA. At lower currents, the LMIS outperforms the ICP source, but imaging resolution below 25 nm has been demonstrated with ICP systems (this compares to <5 nm with LMIS), and indeed many of the figures in this paper were obtained using the Xe-ICP beam for the imaging.

The ICP source uses an external radio frequency antenna to couple energy into a source gas to create a plasma from which ions are extracted; this approach avoids internal cathode erosion, which severely limits the lifetime of other types of plasma ion source.[2] The extracted ions are focused into a fine beam and scanned over the sample in a manner similar to an LMIS FIB, although a three-lens column, rather than the typical two-lens column, is employed to handle the extremely wide beam current range (few pA to >1 μA). The ICP source allows for a broad range of possible ion species, with xenon currently being employed as the milling species of choice due to its high mass and favorable ion source performance parameters. For further details of the technology behind the ICP source, and its comparison to LMIS-based systems, readers are directed to earlier publications.[2–5]

While the FIB's ability to image and mill the region of interest is the key enabler of site-specific sectioning, a number of supporting technologies typically integrated into such systems provide important capabilities that allow the analysis to be completed. These include navigation aids, such as computer aided design (CAD) layer overlay, and *in situ* IR and optical microscopes; beam-induced deposition, which allows localized deposition of protective layers or the addition of conductive/insulating tracks; and beam-induced etching, which can enhance milling rates or increase (or even reduce) selectivity between materials, depending upon the gases used. In addition, application techniques have had to be developed to handle particular challenges that arise when working with the larger sections and disparate material sets—examples being the rocking mill method and mill angle evaluation described in Sec. 3.1.1—and the use of automation recipes to automate or semiautomate some tasks to improve system utilization and improve productivity.

3 Case Studies

A number of case studies will be considered to illustrate key applications to which the plasma-FIB has been employed in the two years since its introduction.[6–14] These are divided into several sections—the first covers TSVs, both filled and open; second, die-to-die bonding is discussed; then die-to-package bonding. In many cases, the plasma-FIB employs other upstream analysis techniques and die/package-level design data to provide important targeting information on where to perform the physical analysis. Such techniques[15] can help locate mechanical or structural issues (e.g., acoustic microscopy) or electrical defects or marginalities [e.g., probing, emission microscopy, scanning electron microscopy (SEM) electron beam absorbed current (EBAC)], or provide information on the 3-D layout of the various interconnected components (e.g., CAD databases; optical, IR, and x-ray microscopes).

The case studies focus on site-specific cross-sections, but it should be noted that the plasma-FIB has been used at other points within the system-level design/debug cycle, such as to create functional prototypes by using the ion beam to add and remove connections at the package level.[10] Such package edit is analogous to circuit-level editing utilized with Ga-FIBs[1] and demonstrates the flexibility and utility of the (plasma) FIB as a tool for supporting the development of new processes and products.

3.1 *TSV*

TSVs are a fundamental building block for many 3-D integration schemes, and so considerable attention has been given to their development. Figure 1 demonstrates the applicability of plasma-FIB for analyzing such samples, where a section >100 by 100 μm was formed in ~42 min of total milling time (beam current range from 1.3 μA to 270 nA). In this case, the section is deeper than needed for the specific TSVs shown to assess the preparation time for a range of TSV heights. Several of the case studies below utilize >100-μm-tall TSVs.

The sample quality is excellent, with minimal mill artifacts (often called curtains) due to the use of the rocking milling method, while the resulting ion beam images show off many of the typical image contrast mechanisms seen when using an FIB (whether using Ga or Xe as the ion) for imaging[1,5]—namely, good materials contrast between different layers; channeling (grain) contrast in metal films; and passive voltage contrast, causing insulating layers to appear dark. Such high-contrast images generally make it straightforward to understand the overall construction and dimensions of the sectioned structure; if higher magnification, or resolution, imaging is required, SEM can also be used (see, for example, Sec. 3.2.3).
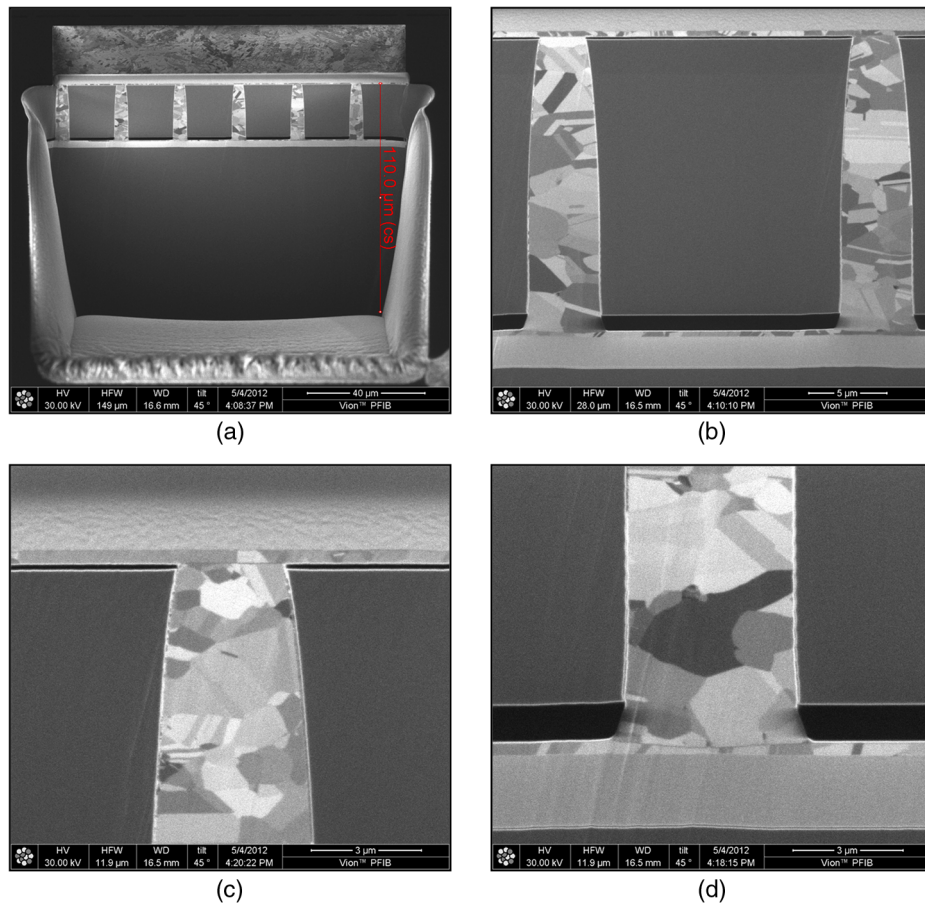
Fig. 1 Plasma-focused ion beams (FIB) milled cross-section of Cu-filled through silicon vias (TSVs)—imaged with the same Xe ion beam. (a) The width and depth is >100 by 100 μm, showing that the section size would have been suitable for much taller TSV stacks as well. Higher magnification views are shown in (b), (c), and (d) (image widths: 140, 28, 12, and 12 μm, respectively). Sample courtesy of SEMATECH.

3.1.1 Grain-structure investigation of filled TSVs

In this case study,[12] plasma-FIB milling was evaluated and optimized for SEM electron backscatter diffraction (EBSD) cross-section analysis of Cu-filled TSV interconnects. For quantitative EBSD grain structure analysis of the Cu filling, it is essential to achieve a perfectly flat cross-section and not to modify the Cu grain structure. Additionally, for small-scaled TSV geometry with high aspect ratios and diameters of <10 μm, an almost perpendicular cross-section through the TSV center is required. Because milling rates do vary locally and massive curtaining may occur, particularly in deep cross-sections, these milling artifacts can make subsequent SEM analyses of the barrier and sidewall isolation as well as the Cu grain structure difficult or even impossible. To overcome this problem, advanced milling strategies based on automated specimen rocking were evaluated and optimized for TSV cross-sectioning. In this study, the surface quality resulting from these new milling strategies was analyzed in detail and evaluated for further EBSD grain structure analyses.

The plasma-FIB milling and EBSD grain structure analyses were investigated using blind TSVs of 50 μm diameter and 150 μm depth, fabricated in 300-μm-thick Si wafers. The specimens were analyzed after Cu filling process (as deposited) and after annealing at 400°C for 3 h in an N$_2$ atmosphere to reveal changes in the Cu microstructure induced by thermal cycling. The test samples were first prepared by cleaving the Si specimen along an array of TSVs. Then, mechanical polishing was used to approach the edge of several TSVs, enabling optimal access for later plasma-FIB processing and for the EBSD analysis.

To minimize curtaining artifacts caused by the surface topography of the TSV prior to plasma-FIB milling, a protective Pt layer was deposited on top. Following this, rapid plasma-FIB milling was performed at each TSV until reaching the center of the TSVs using beam currents of 570 nA for 10 min (step 1) and 230 nA for 7 min (step 2). After this coarse milling, a final plasma-FIB polishing step was additionally performed to improve the surface quality, using different milling parameters on each TSV. These parameters were the beam current (27 or 74 nA), the milling pattern (box or line by line), and the specimen that was polished either in static or in automated rocking mode. In the rocking mode, the specimen is alternating tilted (plus and minus 8 deg) laterally in between the polishing steps (Fig. 2). The benefit of using different tilt angles is that curtaining effects from one direction are removed by the milling from the second direction, resulting in a much smoother section face. It could be shown that the massive curtaining occurring after 27-nA standard perpendicular polishing (~1 μm surface topography) can be removed almost completely (~50 nm surface topography) by further stepwise rocking beam polishing (Fig. 3).
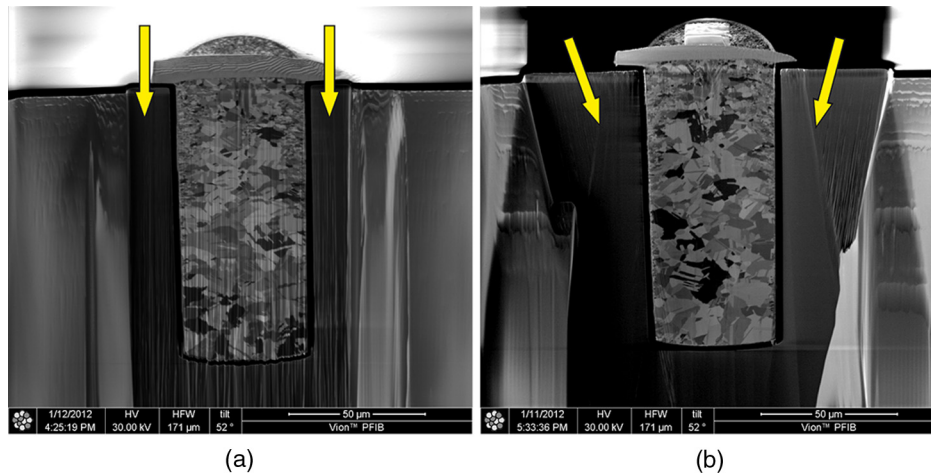
Fig. 2 Plasma-FIB milled cross-section of a Cu-filled TSV after final polishing with 30 keV, 27 nA ion-beam without specimen rocking (a), P-FIB milled cross-section of a Cu-filled TSV after final polishing with 30 keV, 27 nA ion-beam with specimen rocking at ±8 deg (b). (Image widths 170 μm).
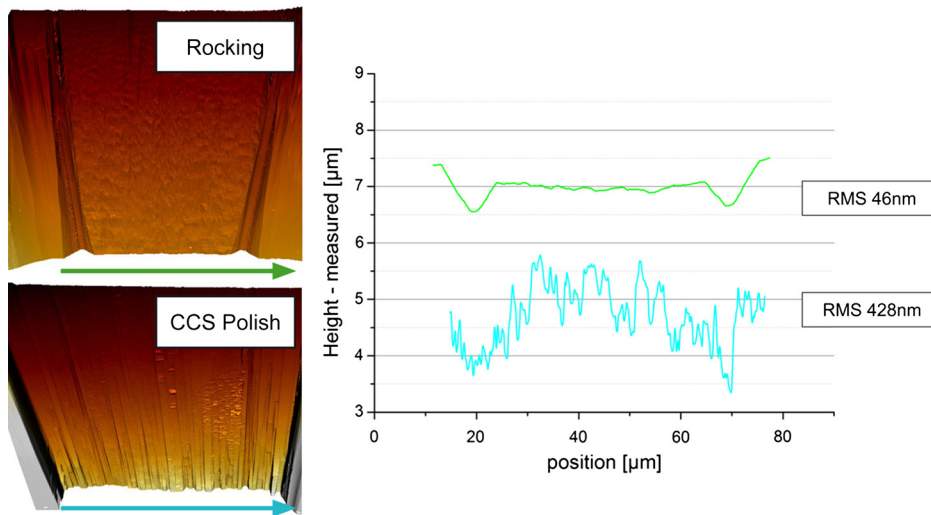

Fig. 3 AFM profile scans across TSV bottom surface polished by rocking beam technique (upper line scan) compared to TSV bottom surface polished by standard cleaning cross-section method (lower line scan).

Additionally, for the different milling regimes, vertical profile line scans along the polished TSV center were measured by AFM to compare the achievable slope angles. For the TSV polished with a 27-nA ion beam current, a slope angle of ~3 deg was measured. This angle was found to be independent from the other milling conditions. The profiles were almost linear. As a result, optimal conditions for TSV cross-sectioning and further EBSD grain structure analysis requiring a low surface roughness could be achieved by 27-nA final polishing applying the rocking/polishing technique—with a 3-deg overtilt included to give a vertical final result.

In order to optimize the TSV processing steps, the relationship between microstructure, e.g., the local texture, and the reliability properties under temperature cycling have to be investigated. EBSD is an efficient and practical technique for grain structure analyses due to its excellent spatial resolution. The specimens were investigated by scanning the electron beam across a selected surface area. Due to the high surface sensitivity of EBSD, the quality of the obtainable results is directly related to the quality of the prepared specimen surface. In this case study, the geometrical requirements for an EBSD analysis could be fulfilled by specific removal of material along the direction of the diffracted beam, enabling an artifact-free texture analysis with spatial resolution in the range of nanometers. Figure 4 shows quantitative EBSD orientation maps of Cu-filled TSV cross-sections made by plasma-FIB. Comparing TSVs as fabricated with additionally annealed TSVs, the change of grain size and grain distribution due to the temperature processing can clearly be obtained.

Overall, it was demonstrated that plasma-FIB milling enables time-efficient grain structure analysis and sidewall characterization of Cu-filled TSV interconnects, offering significant advantages compared to common mechanical or Ga-FIB-based preparations. Furthermore, plasma-FIB polishing provides a fast and reproducible method, which allows cross-sections without significant damage or modification of the microstructure. This is essential for EBSD-based process characterization to study Cu protrusions or other microstructural changes that are related to annealing of TSVs and cause reliability issues.
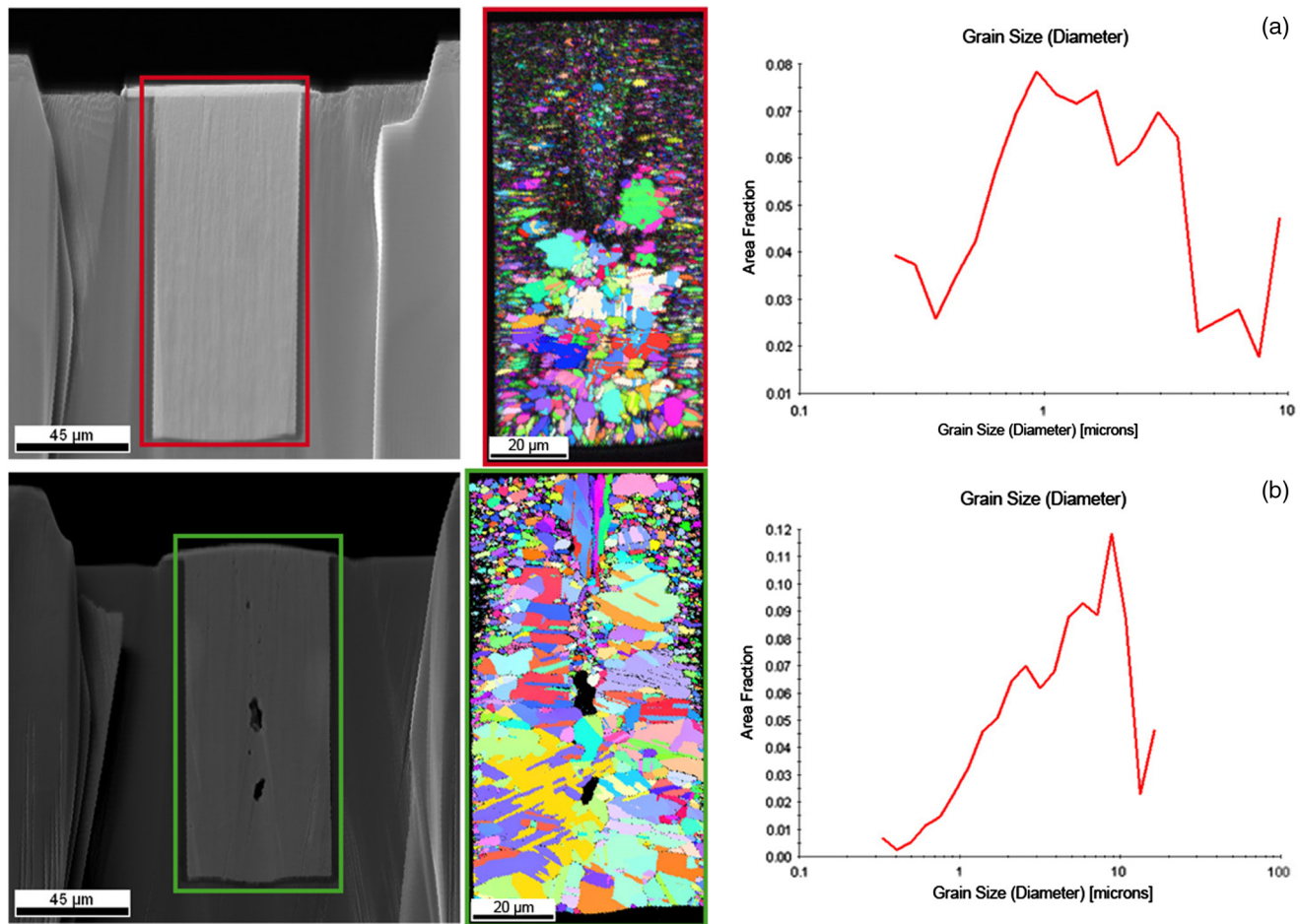
Fig. 4 Electron backscatter diffraction (EBSD) cross-section analysis of the Cu grain structure and grain size distribution. TSV specimen after Cu deposition (a) and after 400°C anneal for 3 h (b). Measurements and calculations are performed using an Oxford Instruments Channel 5 EBSD system.

3.1.2 *Inspection and failure analysis of open TSVs*

A specific open TSV interconnect technology has been developed as an alternative to Cu-filled TSVs. The Bosch etching process combined with further IC processing steps is used to form TSV structures with sidewall isolations and metallization with Ti/TiN, W, and Al. Finally, the TSVs are capped by a silicon dioxide film and silicon nitride layers. For process optimization and failure analysis, the sidewall layer structure has to be imaged and measured. To get access for SEM and TEM imaging, cross-sections of the open TSV structure have to be made. In most cases, wafer cutting through the TSV is not applicable because of the bonded Si/Si oxide/Si substrate. Alternatively, large area mechanical grinding or ion beam polishing can be applied. For precise cross-sectioning to get access to specific TSV areas of interest or to defect sites within the TSV structure, rapid plasma-FIB milling has been evaluated. In a first step, high-current plasma-FIB cross-sectioning followed by rocking beam polishing of the whole TSV structure was applied to get access to the entire sidewall layer. Strong curtaining effects caused by the open TSV geometry could not completely be removed, limiting the SEM inspection of the sidewall layer. An alternative approach would be to fill the TSV structure before milling, but was not attempted.

For failure analysis of sidewall issues, TSV filling would often not be a good option. Geometrical deviations or located electrical shorts at the sidewall have to be directly accessed to allow for site-specific FIB cross-sectioning. Depending on the defect size and position within the TSV, accuracy of the defect localization, and the request for SEM or TEM, the milling strategy has to be adapted. The following examples demonstrate possible preparation flows.

A crucial requirement is the localization of electrical shorts on TSV sidewalls combined with further target preparation via TSV cross-sectioning and high-resolution electron microscopy analysis. In a first case study, electrical shorts of the TSV sidewall metallization to the Si-substrate were localized by EBAC imaging technique[16] (Fig. 5). In this case, a rough cross-section of the TSV was made by mechanical grinding.

Then standard FIB/SEM cross-sectioning was applied to screen through the EBAC spot. A rough inhomogeneous sidewall was present at the TSV bottom with abnormal thickness deviations of the isolation oxide layer between substrate and sidewall metallization. Additionally, inclusive voids were observed at that interface with more or less 3-D Si artifact probably caused by insufficient Si etch process at TSV bottom. A 3-D-formed Si residue was detected within the EBAC active area, Fig. 6. It shorts the substrate with the
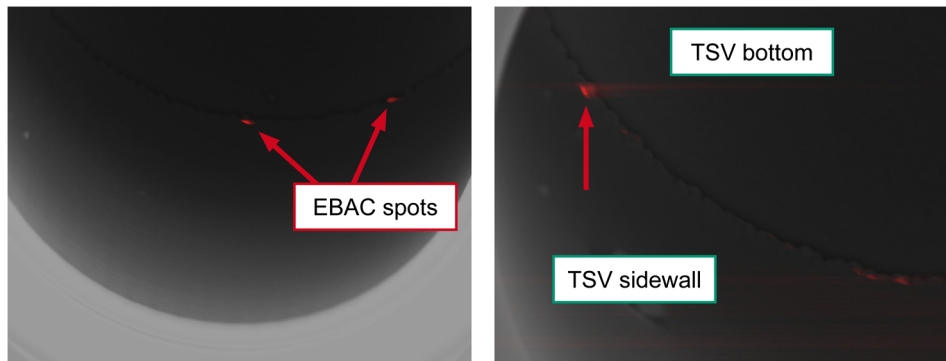
Fig. 5 Overlay of secondary electron (SE) and electron beam absorbed current (EBAC) signals: EBAC analysis on complete TSV structure to localize relevant defect position (red spot) as leaking path.
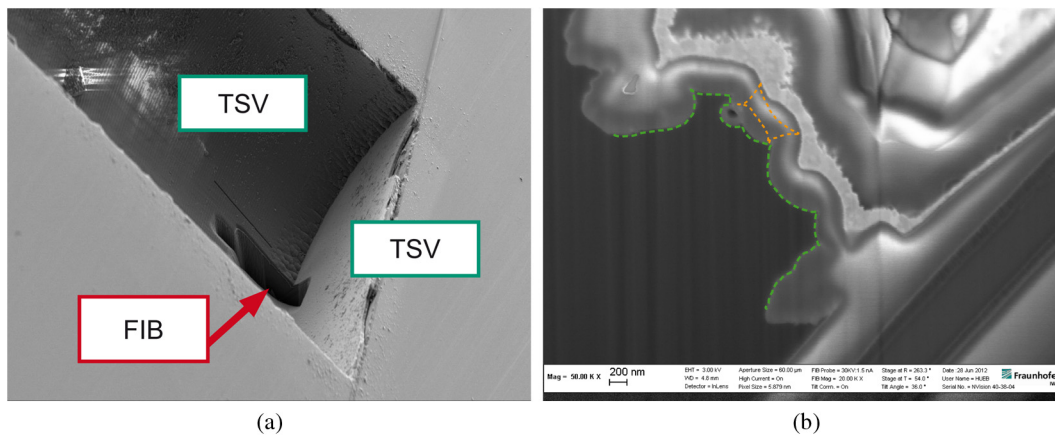

(a)

(b)

Fig. 6 SEM image of tilted sample 45 deg with cross-section at the localized defect position (a). SEM image of cross-section at middle of EBAC spot position after further FIB polishing (b).

TSV metallization at the bottom sidewall, generating a high-ohmic leakage path. Due to its 3-D shape, the complete leakage path was only observable by reviewing several cross-sections. This kind of failure can occur when last Si etch steps were processed insufficiently and, thus, distinctive layer thickness variations were caused. The conducted case study[13] showed the feasibility of these localization and preparation methods to characterize complex 3-D defects at interconnect structures.

A second case study was performed on defective TSV structures with localized delaminated sidewall layers. To find the root cause, the delaminated side wall interface should be analyzed by SEM and TEM imaging. In this case, mechanical grinding was not an option for rough cross-sectioning because of the high risk to fully detach the delaminated sidewall layer. Therefore, rapid plasma-FIB milling with 1.3-μA Xe beam was applied to get a cross-section through the middle of the TSV. A box of $700 \times 300 \ \mu$m and $500 \ \mu$m was milled within only 5 h (Fig. 7).

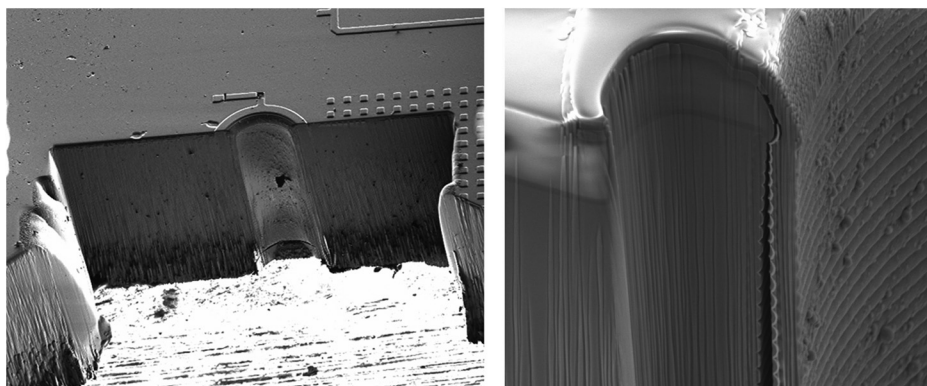Then local sidewall polishing at 70 nA was done at the upper left of the TSV followed by SEM imaging of the

Fig. 7 Plasma-FIB cross-sectioning of an open TSV structure and SEM imaging of the delaminated sidewall layers.
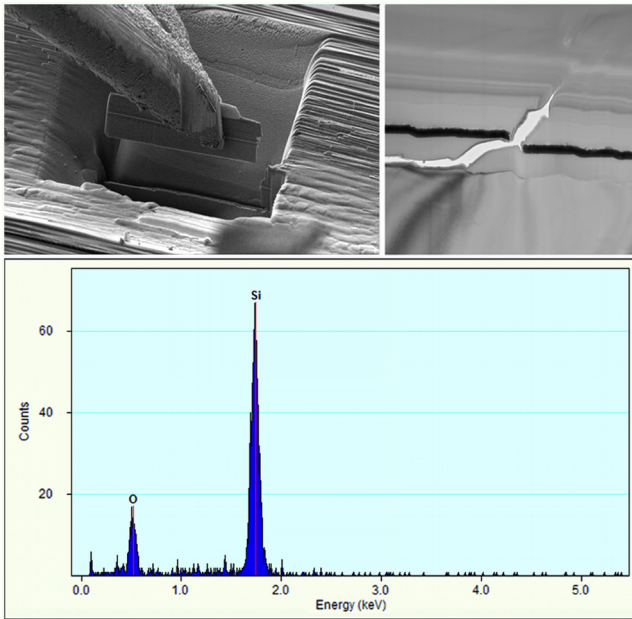
Fig. 8 TEM lamella preparation and imaging of the TSV sidewall with delaminated sidewall layers (top). Energy dispersive spectroscopy measurement at Si-oxide/Si interface showed no contamination detectable (bottom).

delaminated sidewall layer. As a second analysis step, a TEM lamella was made (using a Ga-FIB-based FIB-SEM system) from the plasma-FIB cross-section exactly at the transition between the delaminated and faultless sidewall layer (Fig. 8).

The defect site was analyzed by TEM imaging and energy dispersive spectroscopy (EDS) analysis. A delamination between the Si substrate and the Si oxide isolation could be found, but interface contamination as a possible root cause for a poor adhesion could not be identified, with Si and O being the only significant EDS peaks noted.

3.2 Die-to-Die Interconnects

A fundamental requirement for any 3-D interconnect scheme is a method for connecting the stacked die to each other and/or to any interposers used. Stacking schemes may use a combination of face-to-face, face-to-back, and die-to-interposer bonding, and could also involve a direct connection between the die or include a redistribution layer added to the front/back of the originally manufactured die. Whatever the scheme, there are typically some similar challenges for creating site-specific sections of the interconnects—in particular, locating the area of interest within the stack and then gaining access to the interface in a timely manner, often through a full die thickness. In this section, the plasma-FIB analysis of three die-to-die bonding schemes is discussed.

3.2.1 Face-to-face die bonding

The first example is a face-to-face bonding layout, where a series of Kelvin structures had been created in a reliability test structure. In such a structure, the part of the device stack accessible to the ion beam is the silicon substrate of the upper die. As this is an essentially featureless expanse of polished silicon, the FIB needs an alignment scheme to locate the area of interest. Several methods of navigation are possible, including dead-reckoning from die edges or opening up test holes to orient the sample, but in this example, a more direct and accurate method was employed: using an *in situ* IR microscope to image through the silicon substrate to locate the area of interest [Fig. 9(a)]. For this sample, the die had been polished to 50 μm of silicon substrate remaining. Thicker samples can also be processed—the IR microscope is capable of imaging through full-thickness silicon substrates if necessary—while fast silicon removal with XeF_2 gas etching can be utilized to create a local trench into which the cross-section is then cut. XeF_2 is a common etch gas employed with Ga-FIBs and provides even greater
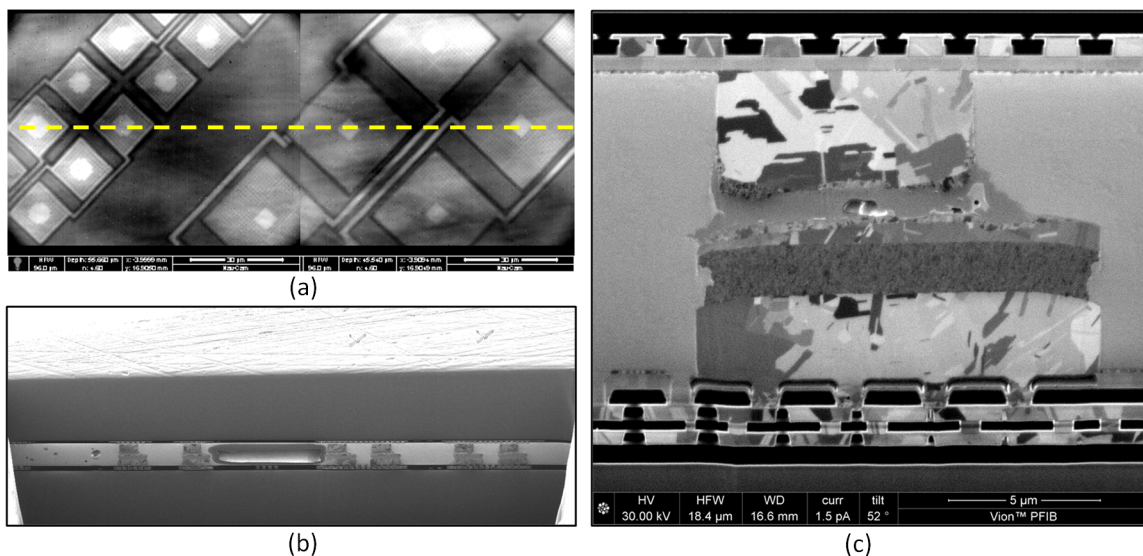

Fig. 9 Cross-section through face-to-face bonded dies. (a) *In situ* IR microscope images were used to locate region of interest through silicon substrate (two images from adjacent areas—total image width 170 μm). The dashed line shows the target position of the section—cutting through 20- and 40-μm-pitch structures. (b) Overview of the cross-section through the microbumps, with void in underfill (image width 250 μm). (c) Detail of one of the 40-μm-pitch interconnect stacks (image width 18.4 μm). Sample courtesy IMEC.
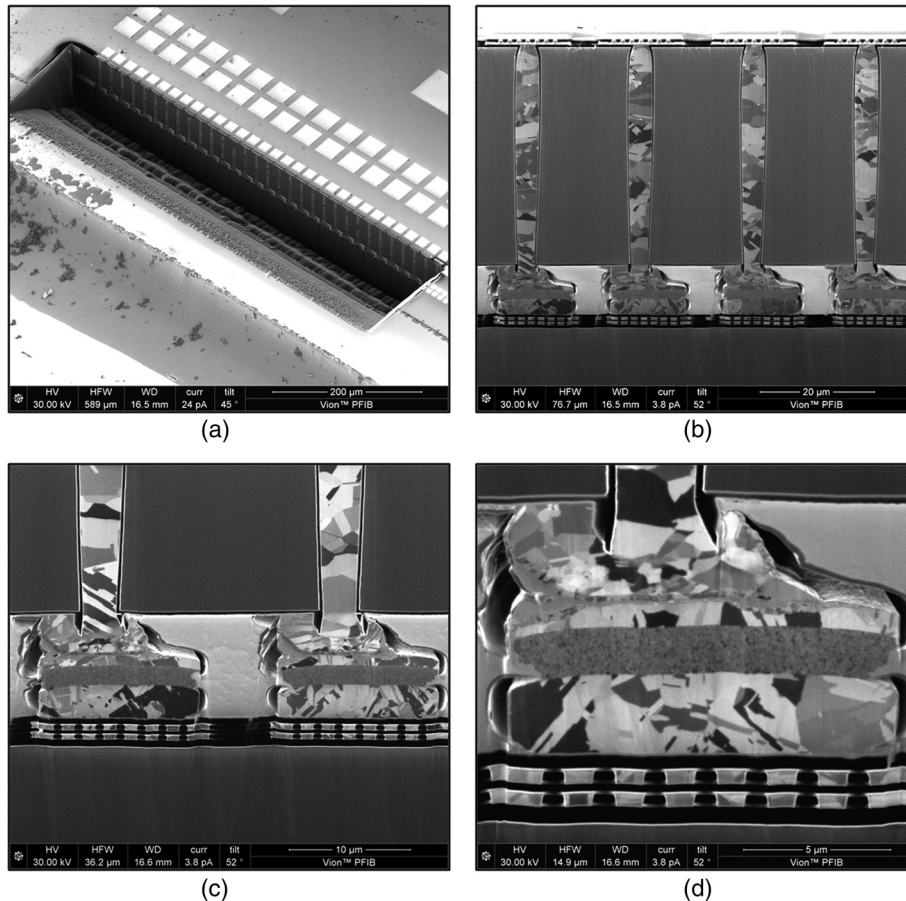
Fig. 10 Cross-section through face-to-back bonded dies. (a) Overview of the complete cross-section through 31 TSVs (image width 590 μm). (b), (c), and (d) Progressively higher magnification views through the TSV array (image widths 77, 36, and 15 μm, respectively). Sample courtesy IMEC.

volume removal rates when combined with the higher currents from the plasma-FIB.[5]

After locating the area of interest in the *in situ* IR microscope, the plasma-FIB preparation took 41 min to expose the section (using beam currents from 1.3 μA to 59 nA) (Fig. 9). Like earlier figures, these images show the utility of ion beam microscopy on the cross-section face. In particular, the different components [intermetallic compounds (IMCs)] that make up the interconnect stack can be observed as layers of differing contrast and grain structure (e.g., large, small, or no grains visible), which will be characteristic of each material composition. By characterizing a comparable device with EBSD or similar technique, a translation from FIB contrast and grain structure to metallurgical composition can often be made, allowing analysis of the bonding process, including layer thicknesses, to be obtained directly from the FIB image.

3.2.2 *Face-to-back die bonding*

Face-to-back bonding schemes incorporating TSVs were also investigated with the plasma-FIB (Fig. 10). Here a series of 31 TSVs and associated die-to-die bonds were sectioned. The sample preparation took ~2.5 h. In a subsequent step, the cross-section face was milled further to expose the next set of TSVs; this took an additional 61 min of milling. The FIB images again show the details of the bonding process as well as some voids in the underfill around the bonds.

Such images could also be used to assess die-to-die alignment or make other critical measurements that can only be assessed once the completed 3-D structure has been assembled. In addition, the localized nature of the sectioning means that multiple sections can be made, even at different angles, which allows more data to be collected from a single device.

3.2.3 *Silicon interposer—burn-in test failure analysis*

The final example in this section is a failure analysis investigation on an interconnect stack that included packaging bump onto a silicon interposer with TSV, which was then microbumped to the lower die (Fig. 11). The sample was part of a reliability burn-in test, and the sectioning was targeted at microbumps thought to be responsible for sample failures.

The main section took <2 h, and when the microbumps were imaged with the FIB, evidence of a problem at one of the interfaces was noted [Fig. 11(c)]. Higher-resolution SEM imaging of a subsequent slice through the defect showed a clear delamination [Fig. 11(d)]. Further delamination examples on other microbumps were also found with the plasma-FIB.

3.3 *Die-to-Package Interconnects*

Strength, quality, and reliability properties of interconnects in microelectronic packaging and microsystem integration
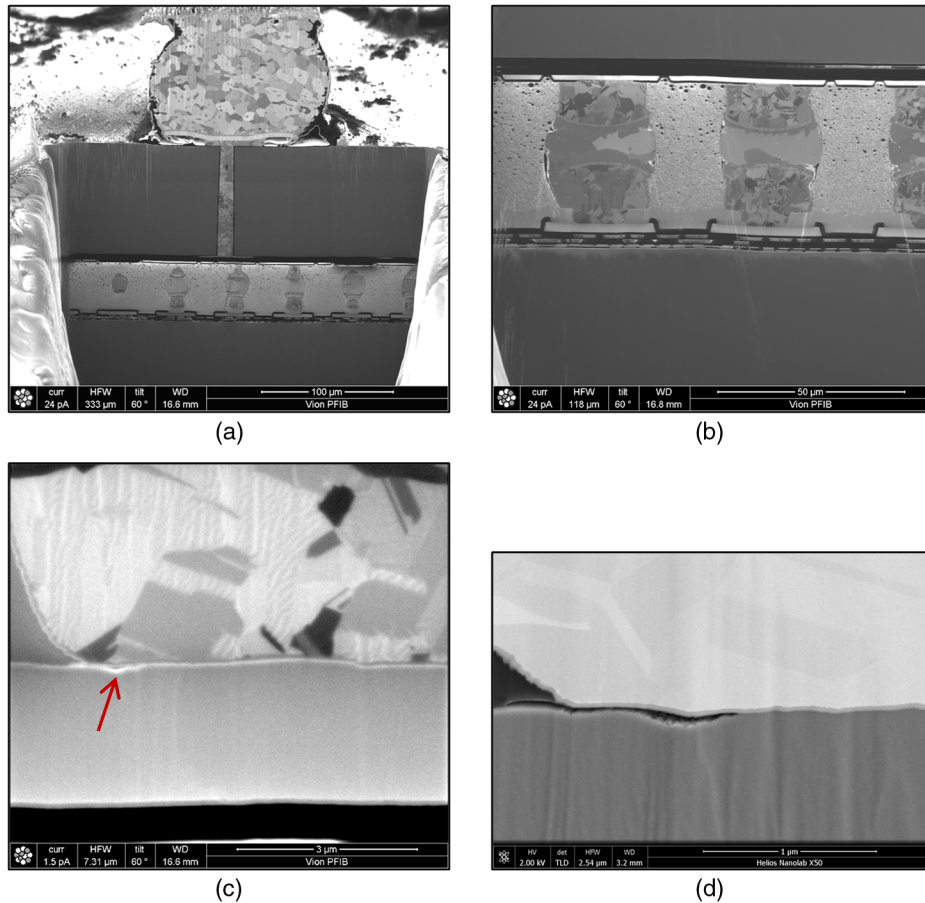
Fig. 11 Die-to-interposer bonding investigation. (a) Overview of the complete cross-section through 31 TSVs (image width 330 μm). (b) Detail of microbumps (image width 118 μm). (c) Plasma-focused ion beam (PFIB) and (d) SEM images of delamination found between bump and underlying (image widths 7.3 and 2.5 μm, respectively).

are closely related to the formation, growth, and physical properties of the different IMCs formed in the interfaces of solder joint contacts. Metallographic grinding techniques are typically used for cross-sectioning to characterize the IMC and interfaces to the upper and lower metallization. But, mechanical grinding could cause artifacts like smearing effects or crack formation caused by the mechanical impact during grinding. Additionally, sometimes it is helpful to access selected solder bump contacts on one device from different directions, which is not possible with mechanical

grinding. FIB preparation provides a very precise navigation to the region of interest by sample imaging. Cross-sections can easily be aligned in different directions, but standard Ga-FIB is typically too slow for such cross-sectioning.

High-current plasma-FIB milling offers a new opportunity to cut through the whole silicon die and solder bump contact without any need of mechanical grinding procedures.[14] In this case, the solder joint contacts have a diameter of 150 μm, which is a typical dimension. As a first step, rapid cross-sectioning was done at highest achievable Xe beam
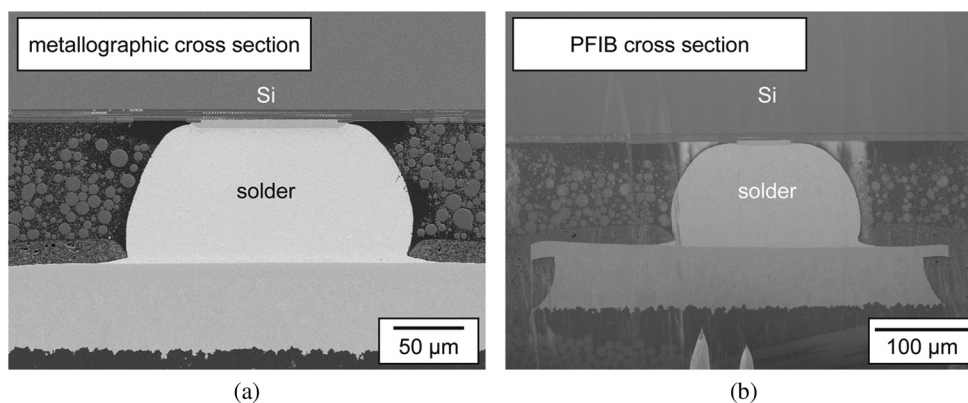

Fig. 12 SEM image of a cross-sectioned solder joint contact shows the remarkable quality of the plasma-FIB prepared area (a) compared to standard metallographic preparation (b).
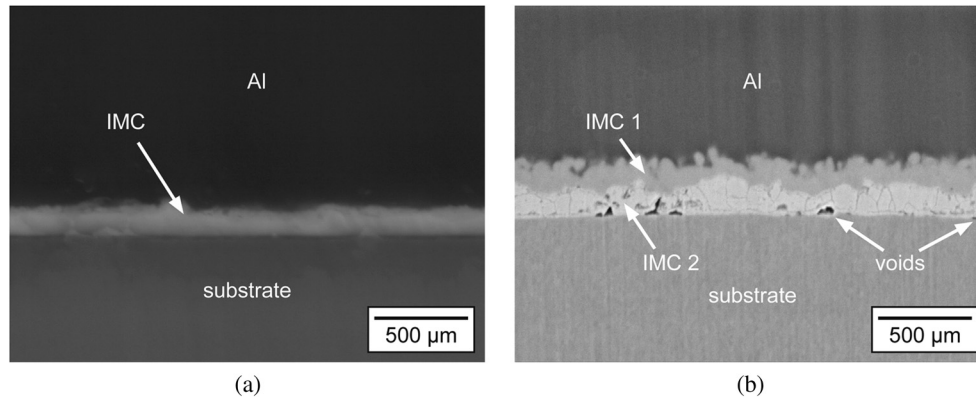
Fig. 13 SEM image of the cross-sectioned heavy wire bond shows the high quality of the plasma-FIB preparation method (b). Separate intermetallics formed in the interconnection region can be observed and failure behavior can be assessed. Using the metallographic procedure (a), the separate intermetallics and void are not detectable due to smearing effects.

current of 1.3 μA. The coarse plasma-FIB milling of a 500-μm-long and 1-mm-deep box takes ~10 h milling time. The final polishing was done by rocking beam milling at ± 8 deg sample tilt by using a 1.3-μA Xe beam.

Figure 12 shows the prepared solder joint contact in comparison to a standard metallographic cross-section. The cross-section surface using plasma-FIB preparation has a remarkable improved quality; nearly no preparation artifacts, e.g., curtaining, are detectable. The microstructural investigations show interface reactions between solder joint contact and under-bump-metallization (see Fig. 13). The under-bump-metallization shows the typical depletion zone of the Ni-P (Ni_3P layer) that occurs because of the interdiffusion of nickel into the Sn solder material and the Ni-Sn IMC formation at this interface, respectively.

In conclusion, it could be demonstrated that the solder joint contact can be accessed by plasma-FIB milling to analyze interface reactions and failure modes, which avoided the artifact generation caused by metallographic grinding.

4 Conclusions

The Ga-FIB has become a critical support tool within semiconductor process and device development over the past 20 years. With the advent of 3-D interconnects, the classical FIB is less well suited due to its low milling speed for the much larger material removal volumes required. This has led to the introduction of plasma-sourced FIBs that extend the material removal rates by some 20 to 50 times. In the two years since their introduction, these plasma-FIBs have demonstrated their capability to extend the site-specific benefits of the FIB technique into the dimension range demanded by 3-D interconnect processes.

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Frank Altmann studied physics at the Technical University Dresden and joined Fraunhofer Institute for Mechanics of Materials Halle (IWMH) in 1996. His research fields are failure analysis on microelectronic devices with respect to high-resolution analytics and defect localization and advanced preparation techniques. He is currently heading the semiconductor diagnostic group at Fraunhofer Center for Applied Microstructure Diagnostics. He is co-organizer of the DACH

focused ion beam (FIB) and further industrial failure analysis workshops. He is author or coauthor of more than 30 publications at academic papers, international conferences, and symposia.

Richard J. Young is strategic technology manager in the Electronics Business Unit at FEI Company, focused on electron and ion beam systems used for pathfinding and process development of advanced semiconductor devices. He joined FEI in 1991 and holds a PhD in physics from the University of Cambridge, where his research included the application of focused ion beams for beam chemistry and for TEM sample preparation. He holds several U.S. patents and has published widely on focused ion beams, SEM, and dual-beam technology and applications.