Holistic lithography and metrology's importance in driving patterning fidelity

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Keynote Presentation

Content

- 43 years overlay metrology in microlithography: How did we get here?
  - Stepper metrology improvements
  - Improved correction potential
  - Extend feedback loop outside stepper
- Holistic Lithography: where we are today
- The future of Holistic lithography: where we are going
- Summary
43 years overlay: 3 orders of magnitude down¹

1973: Introducing the first 1:1 wafer stepper, ~0.5 μm overlay

¹Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015

43 years overlay: 3 orders of magnitude down¹

Transition to reduction steppers
Manual Stepper setup

Automatic Stepper matching setup
Transition from Stepper to scanners, increased correction capability
External Feedback and control

Holistic approach
High order corrections
Integrated metrology
Computational litho
Design for control

Dual stage scanners allowing increased metrology
Integrated Feedback and process control

¹Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015
43 years overlay: 3 orders of magnitude down, Steppers

1979: 4-parameter reticle to wafer diffraction-based alignment

Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015


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43 years overlay: 3 orders of magnitude down, Steppers

1986: 8-parameter alignment

Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015

43 years overlay: 3 orders of magnitude down, Steppers¹

1987-97: Increased correctables on step and scan

Lens complexity 2.6x reduced
Image area 14x reduced¹
Identical exposure field

Step and repeat  Step and scan
The small Step and Scan slit enabled imaging and overlay adjustments on millimeter level by adjusting dose, aberration and slit position during scanning


43 years overlay: 3 orders of magnitude down, Steppers¹

2000: Multi-color alignment increased process robustness

Frank Bornebroek; Jaap Burghoom; James S. Greeneich; Henray J. L. Megens; Danu Satriasaputra; Geert Simons; Sunny Stalnaker; Bert Koek, “Overlay performance in advanced process,” Proc.SPIE vol.4000, Optical Microlitography XIII, Feb 2000

¹Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015
43 years overlay: 3 orders of magnitude down, Steppers¹
2001: Increased metrology time at higher productivity using dual stage


2001: Increased metrology time at higher productivity using dual stage

Dry focus and alignment: additional single stage overhead

Wafer Cycle with dual immersion stage

Swap

Time Line for Wafer Cycle with single immersion stage

Dry metrology

Expose

Unload

Load

Metrology Position

Expose Position

Dry focus and alignment: additional single stage overhead

Wet/dry change combined with stage swap

2007: Small process-compatible alignment markers by self-referencing

Image rotation prisms

(+1,-1)

(+1,-1)

-90°

90°

(+1,-1)

Detector

Source 1


¹Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015
43 years overlay: 3 orders of magnitude down, corrections¹

User-definable correction capability increased ~4 orders of magnitude

¹Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015

1979: Manual stepper setup using verniers on reduction steppers

2.1. Intrafield metrology model

The intrafield metrology equations model the systematic errors sources within the die, i.e., within one image field. We have extended the earlier intrafield model published by MacMillen[1] to include additional lens distortion terms:

\[
\delta x = a_x + (\Delta M/M) x_0 - \theta y_0 + t_1 x_0^2 + t_2 x_0 y_0 - E(x_0^3 + x_0 y_0^2)
\]

\[
\delta y = a_y + \theta x_0 + (\Delta M/M) y_0 + t_1 x_0 y_0 + t_2 y_0^2 - E(y_0^3 + y_0 x_0^2)
\]


3.1. The interfield model

The interfield model is based on the six parameter model of Perloff[2] extended with bow, as suggested by Arnoldi[3] applied for projection aligners. The model, presented here, is somewhat more complex because we use a three axis controlled stage.

\[
\begin{align}
\delta x &= d_{x0} + X_{m1} x_0 + Y_{m1} y_0 + X_{m2} x_0^2 + Y_{m2} y_0^2 + Y_{m3} x_0 y_0 + Y_{m4} y_0^2 + Y_{m5} x_0^2 y_0 + Y_{m6} y_0^3 + Y_{m7} x_0^3 + R_{x0} \\
\delta y &= d_{y0} + X_{m1} y_0 + Y_{m1} x_0 + X_{m2} y_0^2 + Y_{m2} x_0 y_0 + Y_{m3} y_0^3 + Y_{m4} x_0 y_0 + Y_{m5} y_0^4 + Y_{m6} x_0^2 y_0 + Y_{m7} y_0^5 + Y_{m8} x_0^3 + Y_{m9} y_0^6 \\
\end{align}
\]

43 years overlay: 3 orders of magnitude down, corrections
1993: i-line to DUV automated 99-parameter 8-machine matching setup


43 years overlay: 3 orders of magnitude down, corrections\(^1\)
2007: 20-parameter higher-order user-definable corrections per field


\(^1\)Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015
**43 years overlay: 3 orders of magnitude down, feedback**

1993: Stepper external feedback control

![Graph showing overlay results from automatic feedback control](image1)


Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015

**43 years overlay: 3 orders of magnitude down, feedback**

2000: Stepper advanced process control

![Graph showing overlay results from advanced process control](image2)


Advanced Process Control (APC) can be defined as the use of process derived models, equipment models, sophisticated algorithms and signal processing techniques to:

- Optimize exposure tool behavior from empirical data.
- Identify process critical control elements.
- Optimize process response using modeled elements.
- Anticipate and correct for future process drift before lot exposure.
- Maintain "Adaptive" state model elements.

Figure 1: A Feed-Forward Lithography loop anticipates and calculates exposure tool setup parameters before exposure of the lot. Feedback after metrology is used for lot pass/fail gating and to provide adaptive corrections to the feed-forward algorithms.

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43 years overlay: 3 orders of magnitude down, feedback¹

2008: Litho feedforward and feedback control

![Graph showing overlay improvements from 1970 to 2020 with feedback control.](image)

¹Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015

43 years overlay: 3 orders of magnitude down, feedback¹

2012: Small target design allowing on-product targets

![Graph showing overlay improvements from 1970 to 2020 with on-product targets.](image)

¹Overlay data from projection lithography systems presented in SPIE publications 1973 - 2015

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(a) The diffraction efficiencies of the diffracted orders from stacked gratings are a function of the overlay. (b) An example of a 10x10 μm² target with 4 stacked gratings for x- and y-overlay metrology, and (c) the lithographic exposure steps for 1st and 2nd layer showing both a dense structure without open area's, with compatibility to product structures enhanced by sub-segmentation (enlargement).
Content

• 43 years overlay metrology in microlithography: How did we get here?
• Holistic Lithography: where we are today
• The future of Holistic lithography: where we are going
• Summary
1. Advanced lithography (Imaging, overlay and focus)

Design context used to optimize metrology targets and patterning control scheme

2. Metrology

3. Computational lithography

4. Process window enhancement

Stepper set up and layout optimization for maximum process window

5. Process window control

Stepper control through in-process overlay, focus and CD feedback loops window

6. Process window detection

ASML holistic lithography: 6 competences

1) Advanced Lithography: significantly improved on critical parameters both for immersion as well EUV

**Full wafer Focus Uniformity [nm]**

- Ex Factory
- NXT:1980Di systems
- NXT:1970-1980 field upgrades
- Specification

**Matched Machine Overlay [nm]**

- Full wafer, unfiltered, to reference
- NXT:1980Di systems
- EUV: NXE:3300B
- > 1000 wafers per day up to > 80% uptime

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2) Metrology: boosts performance and productivity
Increase metrology accuracy, cut cost of metrology by a factor of 4

<table>
<thead>
<tr>
<th>Detection NA</th>
<th>Application</th>
<th>Productivity</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>YieldStar 250</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.4 NA</td>
<td>2 acquisitions</td>
<td>0.35s</td>
</tr>
<tr>
<td>+1 order and -1 order</td>
<td>3-Layer OVL</td>
<td>3000pts / lot</td>
</tr>
<tr>
<td>425 - 780nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>YieldStar 350</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.9 NA</td>
<td>1 acquisition</td>
<td>0.2s</td>
</tr>
<tr>
<td>+1 order and -1 order</td>
<td>6-Layer OVL</td>
<td>12000pts / lot</td>
</tr>
<tr>
<td>425 – 885nm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Sensor
- New sensor architecture optimized for dedicated High NA µDBO/F detection branch
- Higher µDBO/F magnification
- Parallel 1st order wedge acquisition allowing for High performance / high throughput mode

Illumination
- Increased source power
- Extension to higher wavelength
- Variable spot size selection

3) Computational Lithography: Robust modeling capability
Negative Tone Development (NTD) resist with physical modeling accuracy improved 59%

Model error (simulated CD – wafer CD) comparison between empirical NTD model and physical resist shrinkage model

Representative 2D patterns

Customer's patterns

Empirical NTD resist model does not capture 3 dimensional shrink impact

Physical NTD resist model accounts for 3 dimensional shrink impacting 2D OPC accuracy
4) Process Window Enhancement: EUV optimization over an increasingly large parameter space improves window 27%.

<table>
<thead>
<tr>
<th>Illumination Pupil</th>
<th>CDU (nm)</th>
<th>Pattern placement error (nm)</th>
<th>2x Line Edge Roughness (nm)</th>
<th>Total EPE (nm)</th>
<th>Simulated contour</th>
</tr>
</thead>
<tbody>
<tr>
<td>POR Quasar 25</td>
<td>1.4</td>
<td>1.0</td>
<td>3.9</td>
<td>4.3</td>
<td></td>
</tr>
<tr>
<td>SMO</td>
<td>1.1</td>
<td>0.8</td>
<td>3.4</td>
<td>3.7</td>
<td></td>
</tr>
</tbody>
</table>

\[
\text{Total EPE} = ((\text{CDU})^2 + (\text{PPE})^2 + (2x\text{LER})^2)^{1/2}
\]

EPE: Edge Placement Error determined by combination of CD, pattern placement and Line Edge Roughness.

5) Metrology: >30% improved wafer edge overlay on Memory process stack using integrated and diffraction-based overlay metrology, fingerprint capturing and sampling optimization.

<table>
<thead>
<tr>
<th>Control mode</th>
<th>Full wafer X / Y Overlay (m+3σ)</th>
<th>Wafer Edge X / Y Overlay (m+3σ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stand Alone Image Based Overlay standard sampling</td>
<td>Stand Alone/ Integrated Diffraction Based Overlay &amp; sampling optimization</td>
<td>Stand Alone Image Based Overlay standard sampling</td>
</tr>
<tr>
<td>Layer A</td>
<td>2.7 / 4.5</td>
<td>2.7 / 2.9 (IM)</td>
</tr>
<tr>
<td>Layer B</td>
<td>3.6 / 4.6</td>
<td>2.9 / 4.1 (SA)</td>
</tr>
</tbody>
</table>

>30%
6) Process Window Detection: Engineering efficiency improvement by computational assisted alignment marker, recipe and sampling scheme optimization

Metrology target design for control (D4C¹)

Scanner grid matching

On-product overlay optimization and control

Diffraction Based Overlay

Across platform matching

on-product corrections

\[ I_n = I_n(ov) - 1 + 1 \]

- Target to device matching
- Metrology accuracy

- Overlay grid matching
- Baseline stability control

- Correction model
- Sampling scheme


Content

- 43 years overlay metrology in microlithography: How did we get here?
- Holistic Lithography: where we are today
- The future of Holistic lithography: where we are going
  - Fingerprint estimation and Sampling optimization
  - Target design and recipe optimization
  - Pattern fidelity
- Summary

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Challenges by balancing sampling and correction density
Improved noise suppression by determining fingerprint capture

- Number of litho-compatible parameters is close to or exceeds number of measurements
  → Issue with noise suppression

- Typical number of parameters sufficient to capture fingerprint
  → Optimal noise reduction/fingerprint capture balance

- Not enough parameters for high-resolution litho-compatible fingerprint
  → Issue with fingerprint capture

Fingerprint capturing will improve correction noise

Measured
- Overlay per wafer

Reference
- Average overlay on this location
- Statistical precision

Modeled fit results
- Good model at this location: Fit is within precision of reference
- Not-so-good model: outside precision
- Difference to edge of statistical precision: non-captured fingerprint

Non-captured fingerprint = 0 if model fit is within precision
Fingerprint modeling can decrease # parameters >10x resulting in better capturing the errors and reducing noise.

Total Average Fingerprint

Third order wafer model (55 parameters)

6 parameter correction per expose (~1200 parameters)

Fingerprint model (85 parameters)

Errors not captured by the model

M+3s=3.0 ; 2.7 nm

M+3s=2.3 ; 2.3 nm

M+3s=2.2 ; 2.2 nm

Reducing overlay by 25% and improving edge yield

Using an optimized sampling scheme

Process Of Record models and sampling

Overlay

Higher-order models and optimized sampling

M.S. Kim et al., “Reduction of wafer-edge overlay errors using advanced correction models, optimized for minimal metrology requirements”, SPIE Conference 9780-9, February 2016
Content

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  - Target design and recipe optimization
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Diffraction-based process-robust overlay metrology
Fast and affordable overlay metrology allowing dense wafer sampling

\[ OV = 0: \quad A = I_{+1} - I_{-1} = 0 \]

\[ OV \neq 0: \quad A = I_{+1} - I_{-1} = K \times OV \]

Process-dependent \(K\) factor can be eliminated with 2 “biased” gratings:

- Grating 1: \( A_+ = K(OV + d) \)
- Grating 2: \( A_- = K(OV - d) \)

\[ OV = d \frac{A_+ + A_-}{A_+ - A_-} \]

Accurately determined by mask writer
Accurately measured by YieldStar

Metrology target and recipe design requires optimization to meet tight overlay requirements, computational approach needed to reduce the experimental verification/engineering time.

Using multi-wavelength to improve process robustness on Yieldstar, reducing the influence of process asymmetry on overlay.

Leon Verstappen et al., "Holistic Overlay Control for Multi-patterning Process layers at the 10-nm and 7-nm nodes", SPIE conference 9778-141, Feb 2016
Holistic Metrology Qualification selects recipe with best overlay accuracy

For every point, the overlay is calculated based on multi-wavelength slope:

The overlay maps of individual YS recipes are compared to the self-reference overlay:


Target to Device overlay mismatch reduced to < 0.9 nm

By optimizing target layout compatibility with device layout

J. Zhou, “Eliminating the offset between overlay metrology and device pattern using computational target design” SPIE conference 9778-50, February 2016
Substantial alignment process robustness improvement
Using multiple wavelengths and polarizations in computational overlay simulation

Simulated alignment error [nm]

5x process excursion reduction
2x process robustness reduction

- Current alignment sensor
- + 2 polarizations and improved algorithms
- + intensity information improved algorithms

30 different process stacks and marker combinations in both FEOL and BEOL

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  - Target design and recipe optimization
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- Summary
Pattern fidelity is impacted by multi-patterning and variability

Edge placement error affected by overlay and CD variations

Pattern fidelity affected by CD proximity and pull back

Best pattern fidelity with EUV

ArFi with LE3 after TiN etch

EUV exposed after TiN etch

Data courtesy IMEC 10-nm logic design (M1)

CD variation after etch effectively controlled with scanner

Self-aligned double patterning fidelity optimized by balancing spacers S1 and S2

Litho

HM etch

Spacer deposit

Spacer etch

Trench etch

Litho

Free-form dose control per field

High resolution dose corrections

YieldStar CD metrology

Final Etch
CD fidelity improved by 2x using higher-order corrections

2 wafer data

No spacer control

Spacer control

S1-S2
0.70nm \(\rightarrow\) 0.44nm
47% improved

S1-S2
0.50nm \(\rightarrow\) 0.21nm
58% improved

S1-S2
0.35nm \(\rightarrow\) 0.24nm
31% improved

J. Lee et. al, “Spacer multi-patterning control strategy with optical CD metrology on device structures” SPIE conference 9778-80, February 2016

Challenge in pattern fidelity and control

E-beam inspection (EBI):
- Resolution: 0.5~5 nm
- Throughput: \(\sim\)10⁴ WPH

Bright field inspection (BFI):
- Resolution: \(\sim\)15 nm
- Throughput: \(\sim\)1 WPH

E-beam inspection doesn’t meet productivity requirement

PWO enables hotspot detection with required resolution and productivity and …

Computational patterning fidelity prediction:
- Resolution: <5 nm
- Throughput: \(\sim\)10² WPH

Bright field inspection misses patterning errors when size <15 nm

… hotspot reduction using scanner correction and control
Patterning fidelity litho control impact, the next holistic step
Using computational prediction allowing per wafer patterning control

- Hotspot detection
- Measured product wafer focus & CD
- Computational Patterning fidelity prediction
- Patterning fidelity after scanner control

Tachyon simulations
TwinScan & YieldStar metrology

Source: Imec 10 nm SuperNova M1A

Extension of control loops to patterning and fidelity

- Process aware control
- Process and design aware control
- Lithography

- After litho hotspots
- E-beam validation
- After etch hotspots

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Pattern fidelity improvement through scanner corrections


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Future trends in holistic lithography – overlay

- In general for overlay and pattern fidelity:
  - The stepper correction capability is on a millimeter scale and underutilized
  - Sampling from product vs targets could lead to a different overlay measurement

- What we observe for overlay:
  - Overlay contribution from wafer deformation and marker fidelity vs stepper accuracy is increasing in the total overlay budget
  - Wafer deformation and marker fidelity variation from wafer to wafer starts contributing in the overlay

- As a consequence for overlay:
  - There needs to be a consistent trend down in cost per measurement for metrology to allow higher sampling density
  - Sampling schemes need to be optimized capturing the relevant parameter instability and allow averaging to reduce noise
  - Above will allow scanner correction capability moving from feedback per batch on global targets to feedback per wafer on intra-die product structures

Future trends in holistic lithography – pattern fidelity

- What we observe for pattern fidelity:
  - Multiple patterning complexity increases the pattern variability per wafer not to be captured by existing tools for acceptable cost
  - The variability widens from variability in CD to variability in 3D geometry including edge placement and defects

- Pattern fidelity requirements could be met by:
  - Optical CD metrology allows chip manufacturers to increase sample rate for acceptable cost allowing scanner correction capability per die per wafer
  - Defects could be predicted by simulating hotspots and convolutes with wafer focus, dose and aberration maps producing a per wafer defect probability map
  - Per wafer control loops can be designed for defect and edge placement by driving the stepper settings