Delivering complexity at the frontier of electronics

Mayberry, Michael
Delivering Complexity at the Frontier of Electronics

Mike Mayberry
Director of Components Research
VP, Intel Corporation

September 2013
Complexity Sells

- Enables the impossible to become possible
- Complexity that enables simplicity of use
- Complexity can take many forms (density, structure, data, function, ...) but ultimately people pay for use
- Delivering complexity makes our business go!
“Any sufficiently advanced technology is indistinguishable from magic”
- Arthur C. Clarke 1973

1 x 10^9
1 billion transistors fit into an area of One square centimeter

~1 x 10^18
Intel ships about one quintillion transistors per year

Intel 2013

Every 2 years
Intel delivers a new manufacturing process

2 x Better
than the previous generation

Intel in the Future
We Need Both New Materials & New Structures

Increasing Coupling

"idle power"

Planar With High K

Fins & Multigate

Increasing Mobility

"performance"
(can trade for power)

Strain

PMOS Ieff @ 0.7V (Normalized)

Generation (nm)

Tri gate
Strain
Classic
High Performance Computing Segment Needs
Decades of Performance Increases
FLOPS
Zeta
Exa
Pera
Tera
Giga
Massive computing power to solve complex problems

Crafting Films with Atomic Layer Deposition

Need Multiple Applied Sciences to reap benefits

X-ray
Space Telescope
Multi-layer Coatings

Precision Mirrors

EUV Lithography

Immersion Lithography

Materials Synthesis

Computational Materials

High Performance Computing Segment Needs
Decades of Performance Increases

Source: Intel Unveils Meeting 2020

Weather Forecast

Medical Imaging

Genomic Analysis

Nanostructure Processing

Nanostructure Processing
<table>
<thead>
<tr>
<th>Level of detail</th>
<th>No OPC</th>
<th>Model/Rule based OPC</th>
<th>aggressive OPC + assist features</th>
<th>Inverse lithography</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 billion transistors</td>
<td>60 billion design features</td>
<td>1 trillion mask features</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Model/Rule based OPC
Inverse lithography

Terms of Use: https://www.spiedigitallibrary.org/terms-of-use
The Evolution of PERSONAL COMPUTING

Productivity
80s and 90s

Portability
00s

Ubiquity
10s
What Happens in an Internet Minute?

639,800 GB of global IP data transferred

135 Botnet infections
6 New Wikipedia articles published
1,300 New mobile users
100+ New LinkedIn accounts

47,000 App downloads
204 million Emails sent
583,000 In sales

20 million Photo views
61,141 Hours of music
20 million New victims of identity theft

20 million New Wikipedia articles published
320+ New Twitter accounts
3,000 Photo uploads
3,000 New Twitter accounts

100,000 New tweets
61,141 Hours of music

1,300 New mobile users
100+ New LinkedIn accounts

277,000 Logins
6 million Facebook views
2+ million Search queries

30 Hours of video uploaded
1.3 million Video views

And Future Growth is Staggering

Today, the number of networked devices = the global population
By 2015, the number of networked devices = 2x the global population
In 2015, it would take you 5 years to view all video crossing IP networks each second.
Key Points

• Complexity just from density is insufficient and it has been that way for a decade or more ... increasing value from structure (materials), functions, and data

• Complexity that enables simplicity of use is driving the end market more today than in the past

• Delivering complexity at the right price point makes our business go!
The (likely) near future
Optimizing Choices for Transistors on Multiple Fronts

Increasing COUPLING
(better OFF)

Planar With High K

UTB SOI (or QW)

Fins

Wires/Dots

Increasing MOBILITY
(better ON)

Strain

Ge

III-V

CNT

Graphene
Optimizing Choices for Printed Information

Some useful design
Line Double (& Quadruple)
Dense but low information

High customization

Some useful design

Cost/Vol Tradeoff

EUV
Single exposure limit

193i

Pattern Split

Direct Write

Cost proportional to information
The Gate All Around (GAA) Architecture is the Limit to Structural Electrostatic Control

Source: K. Kuhn et al. TED 59:7 2012
Increasing Capability (Information) of a Single Mask

More printed information for given tool capability

Higher information density

Source: P. Yan, SPEI 2011
Are there fundamental physical limits?

5nm device feature

Vertical devices

III-V Vertical Tunnel FETs

Vertical device structures and new materials

- 5nm device structures have been demonstrated in research labs
- New device architectures are under investigation

Our ability to control is more a limitation than the physics
Control implies we can measure and co-optimize
Managing Material Properties at Nanometer Scale

Grain scattering dominates
Need sub-nm material engineering

Cu wires at 17nm drawn dimension (colors indicate crystal orientation)
Another Sub-nm Example

Pit defect
50 pairs Mo/Si

Bump defect
40 pairs Mo/Si

TEM of 50-pair ML
covered 11nm etched step

Source: Courtesy of SEMATECH
and P. Yan, SPEI 2011
How Small Can We Fabricate and Control?

“Self-Assembling Materials for Lithographic Patterning”
Bill Hinsberg et al, IBM.SPIE 2010

7nm half-pitch
IBM, Park et al, Nanotech 19 2008

Cai et al, Nature July 2010
Control Requires Co-Optimization

Production Share
Has dramatically shifted into captive production

Source: Courtesy of VLSI Research 2013
"The only way of discovering the limits of the possible is to venture a little way past them into the impossible"

- Arthur C. Clarke 1962
Alternative paths

Source: Google Earth

Magic Roundabout
Swindon, UK
Heterogeneous System Integration

Future systems will integrate a much wider variety of materials and device structures

Source: IEDM 2011: The Evolution of Scaling from the Homogeneous Era to the Heterogeneous Era, M. Bohr
Layer Stack Density Benefit: 30-50%

Widespread use requires new design methods ...
... and some new metrology
Beyond CMOS Devices - Noncharge

- Spin Torque Majority Gate (STMG)
- All Spin Logic (ASLD)
- Spin Torque Domain Wall (STT/DW)
- Spin Torque Oscillator (STO)
- Spin Wave Device (SWD)
- Nanomagnetic Logic (NML)

Source: D. Nikonov and I. Young, 2012 IEDM
Exploring Other Ways to Compute Memory & Storage

Fetch & Store

Slower & larger

Faster & smaller

"Von Neumann"

Bottleneck = memory/storage

Transport limited devices make it worse

Compute & Decide

Associate & Decide

Training set

Unknown

Act

Bottleneck = training

Potentially favorable for novel devices

Proc. of SPIE Vol. 8880  888002-26

Downloaded From: https://www.spiedigitallibrary.org/conference-proceedings-of-spie on 06 Jan 2020
Terms of Use: https://www.spiedigitallibrary.org/terms-of-use
The Future of Mask Fabrication?

Massively parallel beam writing
Parallel beam writing
VSB (vector writing)
MEBES (single beam raster)
Key Messages

• Complexity sells ... and thus complexity is your friend
• Novel materials in complex 3D structures are here now and will be increasingly prevalent in the future
• Today we have even more choices than we have had in the past – this is both good and bad
• The future remains bright and masks remain an integral part of our future success
Thank You
Risk Factors

The above statements and any others in this document that refer to plans and expectations for the first quarter, the year and the future are forward-looking statements that involve a number of risks and uncertainties. Words such as “anticipates,” “expects,” “intends,” “plans,” “believes,” “seeks,” “estimates,” “may,” “will,” “should” and their variations identify forward-looking statements. Statements that refer to or are based on projections, uncertain events or assumptions also identify forward-looking statements. Many factors could affect Intel’s actual results, and variances from Intel’s current expectations regarding such factors could cause actual results to differ materially from those expressed in these forward-looking statements. Intel presently considers the following to be the important factors that could cause actual results to differ materially from the company’s expectations.

Demand could be different from Intel’s expectations due to factors including changes in business and economic conditions, including supply constraints and other disruptions affecting customers; customer acceptance of Intel’s and competitors’ products; changes in customer order patterns including order cancellations; and changes in the level of inventory at customers. Uncertainty in global economic and financial conditions poses a risk that consumers and businesses may defer purchases in response to negative financial events, which could negatively affect product demand and other related matters. Intel operates in intensely competitive industries that are characterized by a high percentage of costs that are fixed or difficult to reduce in the short term and product demand that is highly variable and difficult to forecast. Revenue and the gross margin percentage are affected by the timing of Intel product introductions and the demand for and market acceptance of Intel’s products; actions taken by Intel's competitors, including product offerings and introductions, marketing programs and pricing pressures and Intel's response to such actions; and Intel's ability to respond quickly to technological developments and to incorporate new features into its products. Intel is in the process of transitioning to its next generation of products on 22nm process technology, and there could be execution and timing issues associated with these changes, including product defects and errata and lower than anticipated manufacturing yields. The gross margin percentage could vary significantly from expectations based on capacity utilization; variations in inventory valuation, including variations related to the timing of qualifying products for sale; changes in revenue levels; product mix and pricing; the timing and execution of the manufacturing ramp and associated costs; start-up costs; excess or obsolete inventory; changes in unit costs; defects or disruptions in the supply of materials or resources; product manufacturing quality/yields; and impairments of long-lived assets, including manufacturing, assembly/test and intangible assets. The majority of Intel’s non-marketable equity investment portfolio balance is concentrated in companies in the flash memory market segment, and declines in this market segment or changes in management’s plans with respect to Intel’s investments in this market segment could result in significant impairment charges, impacting restructuring charges as well as gains/losses on equity investments and interest and other. Intel's results could be affected by adverse economic, social, political and physical/infrastructure conditions in countries where Intel, its customers or its suppliers operate, including military conflict and other security risks, natural disasters, infrastructure disruptions, health concerns and fluctuations in currency exchange rates. Expenses, particularly certain marketing and compensation expenses, as well as restructuring and asset impairment charges, vary depending on the level of demand for Intel’s products and the level of revenue and profits. Intel’s results could be affected by the timing of closing of acquisitions and divestitures. Intel's results could be affected by adverse effects associated with product defects and errata (deviations from published specifications), and by litigation or regulatory matters involving intellectual property, stockholder, consumer, antitrust and other issues, such as the litigation and regulatory matters described in Intel's SEC reports. An unfavorable ruling could include monetary damages or an injunction prohibiting us from manufacturing or selling one or more products, precluding particular business practices, impacting Intel’s ability to design its products, or requiring other remedies such as compulsory licensing of intellectual property. A detailed discussion of these and other factors that could affect Intel’s results is included in Intel’s SEC filings, including the annual report on Form 10-K for the fiscal year ended December 31, 2012.