

PROCEEDINGS OF SPIE

Design-Process-Technology Co-optimization for Manufacturability IX

**John L. Sturtevant
Luigi Capodieci**
Editors

**25–26 February 2015
San Jose, California, United States**

Sponsored by
SPIE

Cosponsored by
Hitachi High Technologies America, Inc. (United States)

Published by
SPIE

Volume 9427

Proceedings of SPIE 0277-786X, V. 9427

SPIE is an international society advancing an interdisciplinary approach to the science and application of light.

Design-Process-Technology Co-optimization for Manufacturability IX, edited by John L. Sturtevant, Luigi Capodieci,
Proc. of SPIE Vol. 9427, 942701 · © 2015 SPIE · CCC code: 0277-786X/15/\$18 · doi: 10.1117/12.2193828

Proc. of SPIE Vol. 9427 942701-1

The papers included in this volume were part of the technical conference cited on the cover and title page. Papers were selected and subject to review by the editors and conference program committee. Some conference presentations may not be available for publication. The papers published in these proceedings reflect the work and thoughts of the authors and are published herein as submitted. The publisher is not responsible for the validity of the information or for any outcomes resulting from reliance thereon.

Please use the following format to cite material from this book:

Author(s), "Title of Paper," in *Design-Process-Technology Co-optimization for Manufacturability IX*, edited by John L. Sturtevant, Luigi Capodieci, Proceedings of SPIE Vol. 9427 (SPIE, Bellingham, WA, 2015) Article CID Number.

ISSN: 0277-786X

ISBN: 9781628415292

Published by

SPIE

P.O. Box 10, Bellingham, Washington 98227-0010 USA

Telephone +1 360 676 3290 (Pacific Time) · Fax +1 360 647 1445

SPIE.org

Copyright © 2015, Society of Photo-Optical Instrumentation Engineers.

Copying of material in this book for internal or personal use, or for the internal or personal use of specific clients, beyond the fair use provisions granted by the U.S. Copyright Law is authorized by SPIE subject to payment of copying fees. The Transactional Reporting Service base fee for this volume is \$18.00 per article (or portion thereof), which should be paid directly to the Copyright Clearance Center (CCC), 222 Rosewood Drive, Danvers, MA 01923. Payment may also be made electronically through CCC Online at copyright.com. Other copying for republication, resale, advertising or promotion, or any form of systematic or multiple reproduction of any material in this book is prohibited except with permission in writing from the publisher. The CCC fee code is 0277-786X/15/\$18.00.

Printed in the United States of America.

Publication of record for individual papers is online in the SPIE Digital Library.



SPIDigitalLibrary.org

Paper Numbering: Proceedings of SPIE follow an e-First publication model, with papers published first online and then in print. Papers are published as they are submitted and meet publication criteria. A unique citation identifier (CID) number is assigned to each article at the time of the first publication. Utilization of CIDs allows articles to be fully citable as soon as they are published online, and connects the same identifier to all online, print, and electronic versions of the publication. SPIE uses a six-digit CID article numbering system in which:

- The first four digits correspond to the SPIE volume number.
- The last two digits indicate publication order within the volume using a Base 36 numbering system employing both numerals and letters. These two-number sets start with 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B ... 0Z, followed by 10-1Z, 20-2Z, etc.

The CID Number appears on each page of the manuscript. The complete citation is used on the first page, and an abbreviated version on subsequent pages.

Contents

vii	<i>Authors</i>
ix	<i>Conference Committee</i>

INVITED SESSION I

9427 02	The daunting complexity of scaling to 7nm without EUV: pushing DTCO to the extreme (Invited Paper) [9427-1]
---------	--

LAYOUT PATTERNS APPLICATIONS

9427 03	High coverage of litho hotspot detection by weak pattern scoring [9427-2]
9427 04	A pattern-based methodology for optimizing stitches in double-patterning technology [9427-3]
9427 05	Fast detection of manufacturing systematic design pattern failures causing device yield loss [9427-4]
9427 06	Topology and context-based pattern extraction using line-segment Voronoi diagram (Franco Cevina Memorial Best Student Paper Award) [9427-5]

MULTIPATTERNING

9427 07	A systematic framework for evaluating standard cell middle-of-line (MOL) robustness for multiple patterning [9427-6]
9427 08	Self-aligned quadruple patterning-compliant placement [9427-7]
9427 09	Impact of a SADP flow on the design and process for N10/N7 metal layers [9427-8]
9427 0A	An efficient auto TPT stitch guidance generation for optimized standard cell design [9427-9]
9427 0B	Yield-aware mask assignment using positive semi-definite relaxation in LELECUT triple patterning [9427-10]

INVITED SESSION II

9427 0C	DTCO at N7 and beyond: patterning and electrical compromises and opportunities (Invited Paper) [9427-11]
---------	---

LAYOUT OPTIMIZATION AND VERIFICATION I

- 9427 OD **Layout optimization with assist features placement by model based rule tables for 2x node random contact** [9427-28]
- 9427 OE **Standard cell design in N7: EUV vs. immersion** [9427-13]
- 9427 OF **Layout dependent effects analysis on 28nm process** [9427-14]
- 9427 OG **Breaking through 1D layout limitations and regaining 2D design freedom part I: 2D layout decomposition and stitching techniques for hybrid optical and self-aligned multiple patterning** [9427-15]

DESIGN INTERACTION WITH METROLOGY: JOINT SESSION WITH CONFERENCE 9424

- 9427 OH **Full chip two-layer CD and overlay process window analysis** [9427-16]

DFM (DESIGN AND LITHO OPTIMIZATION): JOINT SESSION WITH CONFERENCE 9426

- 9427 OI **Quantitative evaluation of manufacturability and performance for ILT produced mask shapes using a single objective function** [9427-18]
- 9427 OJ **Akaike information criterion to select well-fit resist models** [9427-19]
- 9427 OK **Fast source optimization by clustering algorithm based on lithography properties** [9427-20]

CIRCUIT VARIABILITY

- 9427 OM **Statistical modeling of SRAM yield performance and circuit variability** [9427-22]
- 9427 OO **Layout optimization and trade-off between 193i and EUV-based patterning for SRAM cells to improve performance and process variability at 7nm technology node** [9427-24]

DSA DESIGN FOR MANUFACTURABILITY: JOINT SESSION WITH CONFERENCES 9423 AND 9426

- 9427 OP **Incorporating DSA in multipatterning semiconductor manufacturing technologies** [9427-25]

LAYOUT AND OPTIMIZATION AND VERIFICATION II

- 9427 OQ **Design layout analysis and DFM optimization using topological patterns** [9427-26]
- 9427 OR **Automation for pattern library creation and in-design optimization** [9427-27]
- 9427 OS **A new lithography hotspot detection framework based on AdaBoost classifier and simplified feature extraction** [9427-12]

9427 OT **A methodology to optimize design pattern context size for higher sensitivity to hotspot detection using Pattern Association Tree (PAT) [9427-29]**

POSTER SESSION

9427 OU **20nm CMP model calibration with optimized metrology data and CMP model applications [9427-30]**

9427 OV **Topography aware DFM rule based scoring for silicon yield modeling [9427-31]**

9427 OW **A compact model to predict pillar-edge-roughness effects on 3D vertical nanowire MOSFETs using the perturbation method [9427-32]**

9427 OX **Efficient etch bias compensation techniques for accurate on-wafer patterning [9427-33]**

9427 OY **An efficient lithographic hotspot severity analysis methodology using Calibre pattern matching and DRC application [9427-34]**

9427 OZ **A holistic methodology that drives to process window entitlement and its application to 20nm logic [9427-35]**

9427 10 **Practical DTCO through design/patterning exploration [9427-36]**

9427 11 **Comparison of OPC job prioritization schemes to generate data for mask manufacturing [9427-37]**

9427 12 **VLSI physical design analyzer: a profiling and data mining tool [9427-38]**

9427 13 **The cell pattern correction through design based metrology [9427-39]**

9427 14 **Breaking through 1D layout limitations and regaining 2D design freedom part II: stitching yield modeling and optimization [9427-40]**

9427 15 **Automatic DFM methodology for bit-line pattern dummy [9427-41]**

Authors

Numbers in the index correspond to the last two digits of the six-digit citation identifier (CID) article numbering system used in Proceedings of SPIE. The first four digits reflect the volume number. Base 36 numbering is employed for the last two digits and indicates the order of articles within the volume. Numbers start with 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B...0Z, followed by 10-1Z, 20-2Z, etc.

Adam, Kostas, 10	Gutwin, Paul, 02
Arikati, Srin, 0A	Hamouda, Ayman, 0X, 0Z
Aytuna, Burak, 0U	Han, Daehan, 13
Badr, Yasmine, 0P	Han, Ting, 14
Bahnas, Mohamed, 10	Hashimoto, Takaki, 0K
Bahr, Mohamed, 15	Hong, Aeran, 13
Batarseh, Fadi, 12	Hong, Chuyang, 0W
Bömmels, Jürgen, 0C	Hong, Hyeongsun, 13
Brunet, Jean-Marie, 03	Hong, Lin, 0Y
Burbine, Andrew, 0J	Hong, Sid, 0R
Capodiec, Luigi, 04, 0Q, 0T, 12	Hsu, Stephen, 0Z
Casati, Nathalie, 06	Huang, Jason, 0F, 0R
Chang, Jinman, 13	Hui, Colin, 0U, 0V
Chava, Bharani, 09, 0C, 0E	Hurat, Philippe, 0F
Cheilaris, Panagiotis, 06	Jantzen, Kenneth, 11
Chen, Yijian, 0G, 0M, 0W, 14	Jin, Gyoyoung, 13
Cheng, Qi, 0M, 0W	Jun, Jinhyuck, 0D
Choi, Bumjin, 13	Kallungal, Chidam, 0I
Choi, Heon, 0I	Kang, Jae-hyun, 03
Choi, Junghoe, 0D	Kang, Jinyoung, 13
Choi, Soo-Han, 0A	Katakamsetty, Ushasree, 0U, 0V
Chu, Albert, 02	Kim, Min-Soo, 0O
Cilingir, Erdem, 0A	Kim, NamJae, 03
Cline, Brian, 07	Kim, Stephen, 11
Cote, Michel, 0F	Kim, Taeheon, 13
Crouse, Michael, 0Z	Kim, Taehoon, 0D
Culp, James, 10	Kim, Yonghyeon, 13
Dai, Vito, 04, 0Q	Kodama, Chikaaki, 08, 0B
Debacker, Peter, 0E	Kohira, Yukihide, 0B
Dechene, Dan J., 0Z	Koli, Dinesh, 0U
Deng, ZeXi Rock, 0R, 0Y	Kotani, Toshiya, 08, 0K
Dey, Sandeep Kumar, 06	Krishnamoorthy, Karthik N., 0Q
Ding, Hua, 0F, 0R	Kwan, Joe, 03
Do, Munhoe, 0D	Kwon, Steve, 03
Du, ChunShan, 0Y	Lafferty, Neal, 10
Dusa, Mircea, 0E, 0O	Lai, Ya-Chieh, 0F, 0Q, 0R
ElManhawwy, Wael, 03	Lamba, Gurpreet Singh, 10
Elsaid, Ahmad, 0E	Le Denmat, Jean-Christophe, 05
Endo, Toshikazu, 10	Lee, Dongchan, 0D
Feldman, Nelly, 05	Lee, Joosung, 13
Fryer, David, 0J	Lee, Jooyoung, 13
Gabrani, Maria, 06	Lee, Kweonjae, 13
Gao, Jih-Rong, 0S	Lee, Kyupil, 13
Gerousis, V., 09	Lee, Kyusun, 13
Ghulghazaryan, Ruben, 0U	Leray, Philippe, 0C
Gillijns, Werner, 09, 0E	Lewis, Travis, 11
Gronlund, Keith, 0Z	Li, Helen, 0F
Gupta, Puneet, 0P	Li, Pengcheng, 0Z
Gupta, Rachit, 0H	Liebmann, Lars, 02

Liu, Hongyi, 0G, 14	Thean, Aaron, 0C, 0O
Luk-Pat, Gerard, 0D	Togawa, Nozomu, 0K
Ma, Yuansheng, 0P	Tökei, Zsolt, 0C
Madhavan, Sriram, 04, 0T, 12	Torres, J. Andres, 0P
Madkour, Kareem, 03	Tripathi, Vikas, 0V
Mallik, Arindam, 0C	Trivkovic, Darko, 09, 0E, 0O
Matsui, Tomomi, 0B	Trong, Huynh Bao, 0C
Matsunawa, Tetsuaki, 0S	Vallet, Michel, 05
McGinty, Chris, 10	Vandewalle, B., 09
McIntyre, Gregory R., 09, 0C	Veeraraghavan, Vijay, 11
Meiring, Jason, 10	Verkest, Diederik, 09, 0C, 0E, 0O
Mercha, Abdelkarim, 09, 0C, 0E, 0O	Verma, Piyush, 0T, 12
Miloslavsky, Alex, 0D	Wang, Jinyan, 0R, 0Y
Mitra, Joydeep, 0P	Wang, Lynn T.-N., 04
Mocuta, Dan, 0O	Wang, Pu, 0W
Mountsier, Tom, 0O	Wang, Wei-long, 0I
Nakajima, Fumiharu, 08	Wawrzynski, Glenn, 10
Nakayama, Koichi, 08	Wilson, Jeff, 0U
Nojima, Shigeki, 08, 0B, 0K	Wong, Waisum, 0F
O'Neill, Joseph, 10	Xu, Ji, 0Q
Pack, Robert C., 12	Xu, Wei, 0F
Paek, Seung Weon, 03	Xu, Xiaoqing, 07
Pan, David Z., 07, 0S	Yanagisawa, Masao, 0K
Papadopolou, Evanthia, 06	Yang, Hyunjo, 0D
Park, Chanha, 0D	Yeo, Sky, 0U, 0V
Park, Jinho, 03	Yeom, Kyehee, 13
Park, Minwoo, 0D	Yeric, Greg, 07
Park, Minyoung, 11	Yesilada, Emek, 05
Pathak, Piyush, 0T	Yim, Donggyu, 0D
Raghavan, Praveen, 09, 0C, 0E	Yu, Bei, 07, 0S
Riewer, Olivia, 05	Zhang, Gary, 0Z
Rio, David, 0E	Zhang, LiGuo, 0Y
Ronse, Kurt G., 09, 0C	Zhang, Mealie, 0F
Russell, Gordon, 11	Zhang, Yifan, 0F, 0R
Ryckaert, Julien, 09, 0C, 0E, 0O	Zhou, Jun, 0G, 14
Sakanushi, Keishi, 0K	Zou, Elain, 0R
Sakhare, Sushil S., 0C, 0O	
Salama, Mohamed, 0X	
Samboju, Nagaraj Chary, 0A	
Schuddinck, Pieter, 0C	
Schumacher, Dan, 10	
Shafee, Marwah, 03	
Shang, Shumay, 0H	
Sherazi, S. M. Y., 09	
Sherazi, Yasser, 0C, 0E	
Shokeen, Lalit, 0Z	
Simmons, Mark, 11	
Somani, Shikha, 0T, 12	
Song, Huiyuan, 0F	
Steegen, An, 0C	
Sturtevant, John, 0H, 0J, 10	
Suzor, Christophe, 05	
Sweis, Jason, 0Q, 0R	
Takahashi, Atsushi, 0B	
Talluto, Salvatore, 05	
Tanaka, Satoshi, 0B	
Tawada, Masashi, 0K	
Teoh, Edward, 0Q	
Terry, Mark, 0Z	

Conference Committee

Symposium Chair

Mircea V. Dusa, ASML US, Inc. (United States)

Symposium Co-chair

Bruce W. Smith, Rochester Institute of Technology (United States)

Conference Chair

John L. Sturtevant, Mentor Graphics Corporation (United States)

Conference Co-chair

Luigi Capodieci, GLOBALFOUNDRIES Inc. (United States)

Conference Program Committee

Robert Aitken, ARM, Inc. (United States)

Jason P. Cain, Advanced Micro Devices, Inc. (United States)

Fang-Cheng Chang, Cadence Design Systems, Inc. (United States)

Lars W. Liebmann, IBM Corporation (United States)

Ru-Gun Liu, Taiwan Semiconductor Manufacturing Company Ltd.
(Taiwan)

Mark E. Mason, Texas Instruments Inc. (United States)

Andrew R. Neureuther, University of California, Berkeley
(United States)

Shigeki Nojima, Toshiba Corporation (Japan)

David Z. Pan, The University of Texas at Austin (United States)

Chul-Hong Park, SAMSUNG Electronics Company, Ltd.
(Korea, Republic of)

Michael L. Rieger, Synopsys, Inc. (United States)

Vivek K. Singh, Intel Corporation (United States)

Chi-Min Yuan, Freescale Semiconductor, Inc. (United States)

Session Chairs

1 Invited Session I

John L. Sturtevant, Mentor Graphics Corporation (United States)

Luigi Capodieci, GLOBALFOUNDRIES Inc. (United States)

- 2 Layout Patterns Applications
 John L. Sturtevant, Mentor Graphics Corporation (United States)
 Luigi Capodieci, GLOBALFOUNDRIES Inc. (United States)

- 3 Multipatterning
 Lars W. Liebmann, IBM Corporation (United States)
 Shigeki Nojima, Toshiba Corporation (Japan)

- 4 Invited Session II
 Robert Aitken, ARM, Inc. (United States)
 Michael L. Rieger, Synopsys, Inc. (United States)

- 5 Layout Optimization and Verification I
 Robert Aitken, ARM, Inc. (United States)
 Michael L. Rieger, Synopsys, Inc. (United States)

- 6 Design Interaction with Metrology: Joint Session with Conference
 9424
 Alexander Starikov, I&I Consulting (United States)
 Jason P. Cain, Advanced Micro Devices, Inc. (United States)

- 7 DFM (Design and Litho Optimization): Joint Session with Conference
 9426
 Jongwook Kye, GLOBALFOUNDRIES Inc. (United States)
 Andrew R. Neureuther, University of California, Berkeley
 (United States)

- 8 Invited Session III
 Chi-Min Yuan, Freescale Semiconductor, Inc. (United States)
 Ru-Gun Liu, Taiwan Semiconductor Manufacturing Company, Ltd.
 (Taiwan)

- 9 Circuit Variability
 Chi-Min Yuan, Freescale Semiconductor, Inc. (United States)
 Hsu-Ting Huang, Taiwan Semiconductor Manufacturing Company,
 Ltd. (United States)

- 10 DSA Design for Manufacturability: Joint Session with Conferences
 9423 and 9426
 Michael A. Guillorn, IBM Thomas J. Watson Research Center
 (United States)
 Sachiko Kobayashi, Toshiba Corporation (Japan)
 Vivek K. Singh, Intel Corporation (United States)

- 11 Layout and Optimization and Verification II
Luigi Capodieci, GLOBALFOUNDRIES Inc. (United States)
Chul-Hong Park, SAMSUNG Electronics Company, Ltd.
(Korea, Republic of)
David Z. Pan, The University of Texas at Austin (United States)

