# **Progress in EUV lithography toward manufacturing**

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# ABSTRACT

In this article the recent progress in the elements of EUV lithography is presented. Source power around 205W was demonstrated and further scaling up is going on, which is expected to be implemented in the field within 2017. Source availability keeps improving especially due to the introduction of new droplet generator but collector lifetime needs to be verified at each power level. Mask blank defect satisfied the HVM goal. Resist meets the requirements of development purposes and dose needs to be reduced further to satisfy the productivity demand. Pellicle, where both the high transmittance and long lifetime are demanded, needs improvements especially in pellicle membrane. Potential issues in high-NA EUV are discussed including resist, small DOF, stitching, mask infrastructure, whose solutions need to be prepared timely in addition to high-NA exposure tool to enable this technology.

Keywords: EUV lithography, EUV source, collector, EUV mask, EUV pellicle, high-NA EUV

# **1. INTRODUCTION**

As EUV starts to be used in developing next generation devices, its superiority over ArF-i multiple patterning was verified in many aspects<sup>1</sup>. From design side EUV provides better pattern fidelity as shown in Figure 1, which allows higher design flexibility, better performance, and scalability. In manufacturing point of view EUV reduces the number of masks and in case of logic devices 7nm-node requires even smaller number of masks than 10nm-node, which can reduce both cost and TAT, and contribute to improving yield as a consequence. In order to take advantage of these benefits of EUV, each element of EUV lithography has been thoroughly developed for a long time. In the following sections the recent progresses are reviewed with indications of further improvements.

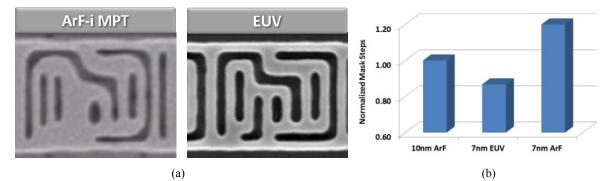


Figure 1. (a) Standard cell pattern of Metall layer in 7nm logic patterned by ArF-i multiple pattering and EUV single exposure, respectively, (b) Comparison of the number of masks(normalized) in 10nm logic by ArF-i multiple pattering, 7nm logic by EUV single exposure, and ArF-i multiple patterning.

Extreme Ultraviolet (EUV) Lithography VIII, edited by Eric M. Panning, Kenneth A. Goldberg, Proc. of SPIE Vol. 10143, 1014306 · © 2017 SPIE · CCC code: 0277-786X/17/\$18 · doi: 10.1117/12.2264043

# 2. EUV EXPOSURE TOOL

### 2.1 Source

There was a rapid improvement in source power since the last quarter of 2016 as shown in Figure 2. A high enough  $CO_2$  power was available at the middle of 2016 but due to the huge gain of this system just a small amount of scattering source has made a huge impact. But recently it began to be successfully controlled and EUV power of around 205W could be demonstrated<sup>2</sup>. More than 250W is forecasted to be demonstrated and expected to be available in the field within 2017.

Although EUV source power depends on collector reflectivity, EUV pulse energy should be maintained uniform. Figure 3 shows the daily trend of EUV pulse energy in NXE3350 system, which corresponds to source power of around 130W in regard to clean collector.

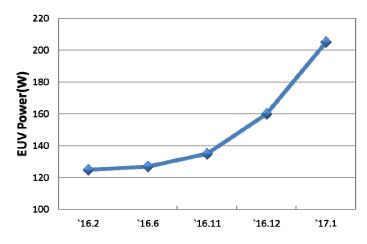


Figure 2. Recent trend of EUV source power scaling-up

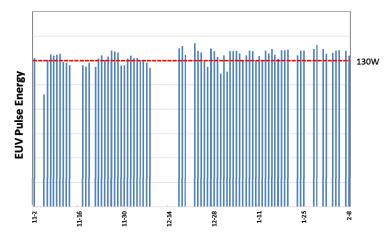


Figure 3. Stability of EUV pulse energy in NXE3350

### 2.2 Collector lifetime

Collector lifetime has been one of the main contributors of availability loss in EUV source. Figure 4 shows the collector reflectivity trend of NXE3300 and NXE3350 over pulse usage. In case of NXE3300 the collector contamination rate was improved from around 1%/Bpulses to 0.5%/Bpulses by optimizing hydrogen flow and vessel temperature. NXE3350 shows similar trend just after installation, but it needs to be improved less than 0.1%/Bpulses before production starts.

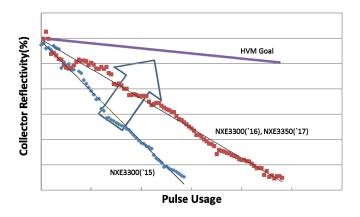


Figure 4. Collector contamination rate of NXE3300 in 2015/ 2016 and NXE3350 in 2017

### 2.3 Droplet generator lifetime

Droplet generator lifetime was improved significantly since droplet generator bundle3 was introduced. Previously droplet generator was the biggest cause of availability loss but now it's just slightly higher than 2% as depicted in Figure 5. The remaining step would be reducing the tin reload time and introducing continuous tin refill technology.

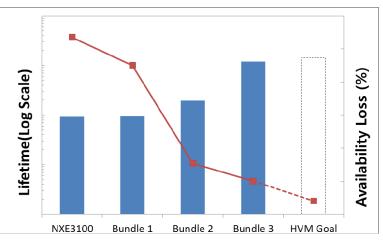


Figure 5. Droplet generator lifetime and its impact on availability loss

### 2.4 Availability

Figure 6 shows the weekly availability trend of both NXE3300 and NXE3350. Average availability of NXE3300 is around 75% and NXE3350 demonstrates better availability than NXE3300 from the early stage of operation.

In order to increase the availability further, improving of collector lifetime is the top priority.

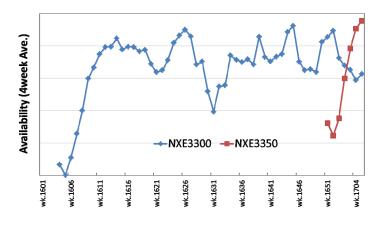


Figure 6. Availability trend of NXE3300 and NXE3350

### 2.5 Scanner Defectivity

Comparing the elements of scanner defects between NXE3300 and NXE3350 there were observed some differences. As described in Figure 7, defects generated from reticle are not seen in NXE3350, which was achieved by implementing various solutions to prevent reticle's hitting safety chuck when EMO happens. It turned out that defects in NXE3350 mainly come from scanner building materials. Although repeated flushing would remove those defects, procedure of fabricating parts and cleaning during integration of scanner need to be improved so that defectivity satisfies the specification and production starts just after installation. The fundamental issue in scanner defect is that the hydrogen flow is directed from optics toward reticle and in the design of the next generation tool protection of reticle from defect should be considered more thoroughly.

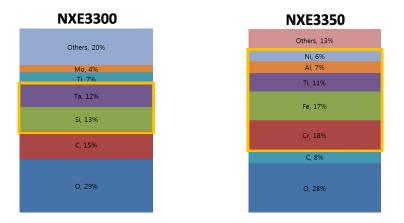


Figure 7. Defect composition of NXE3300 and NXE3350

### 2.6 Imaging

There were several kinds of improvement in the NXE3350 optics like increase of transmittance, decrease of reflectivity for out of band radiation, and reduction of aberration. Figure 8 shows the improvement of the thru-slit CDU as a

consequence of the reduced aberration in NXE3350 system. The mask CD was not subject to OPC in order to compensate the shadowing effect.

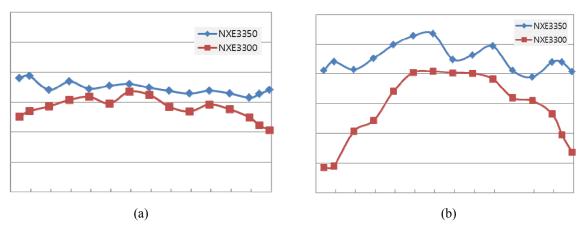


Figure 8. Thru-slit CD Uniformity of horizontal dense line(a) and horizontal iso-line(b) in NXE3300 and NXE3350

# 3. MASK

#### 3.1 Blank multilayer defect

In case the number of blank multilayer defect is less than 5, nearly100% of the defect-free mask yield can be achieved according to defect mitigation simulation for most layers of logic devices. End of last year, most qualified blanks began to satisfy this goal. However sometimes defect mitigation fails even with blanks satisfying the above specification, which is due to inaccurate identification of defect size. As a result each and every defect needs to be reviewed after inspection to measure defect size precisely.

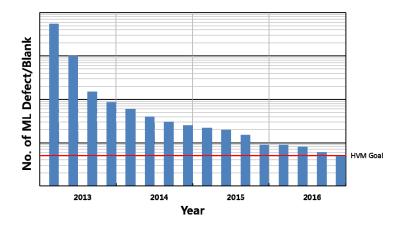


Figure 9. Blank multilayer defect trend

#### 3.2 Actinic mask review system

Samsung developed an in-house actinic review tool using high-harmonic EUV source, zoneplate optics, and scanning microscopy called EMDRS(EUV Mask Defect Review System) as seen in Figure 10<sup>3</sup>. Since then there were continuous

improvements in image performance, which was achieved by enhancing the diffraction efficiency of zoneplate optics and EUV source power. And now this tool shows good enough image quality to be used for 7nm logic production. Since in some cases mask SEM is not able to verify the success of defect mitigation due to its inability to detect phase defects, the actinic mask review tool is indispensable.

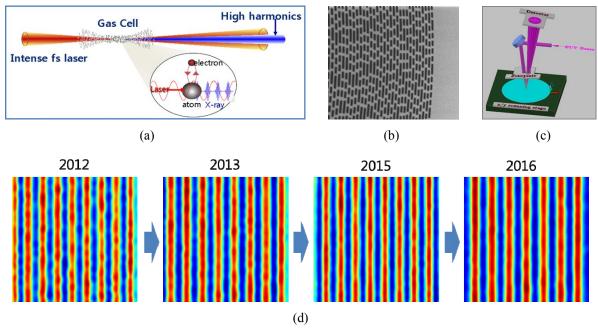


Figure 10. Actinic mask review system

### 3.3 Pellicle

Even when scanner defectivity is below the specification, ideally pellicle is needed in order to prevent the yield loss due to repeating defect from reticle. The most important requirements in EUV pellicle are to have an enough lifetime at high power and a high transmittance<sup>4</sup>. In principle the pellicle for high EUV power would be achievable if the metallic layer

thickness is increased in order to keep the temperature less than 400°C where the pellicle is proved to be sustainable at the expense of transmittance loss as depicted in Figure 11. The material and structure of pellicle membrane need to be optimized to enhance the emissivity at IR wavelength and transmittance at EUV. Figure 12 shows the CD error against the size of particle in the pellicle. Since the smaller pupil fill ratio has the higher sensitivity to particle size, pellicles with different defect quality can be allocated to reticles according to the illumination condition before pellicle yield is matured.

### 3.4 Mask lifetime

After exposure of around 40,000 wafers at NXE3300, bulge defects were observed as shown in Figure 13. The reflectivity was measured after the bulge was broken and it was more than 62% which implies the bulged was Rucapping layer. This kind of phenomena is quite common in EUV optics used under hydrogen environment. By the highly energetic EUV photon hydrogen radicals are generated, which penetrate into the interlayer, recombine, and cause bulges. In order to extend mask lifetime a solution like adding a layer which prevent the penetration of hydrogen radical is needed.

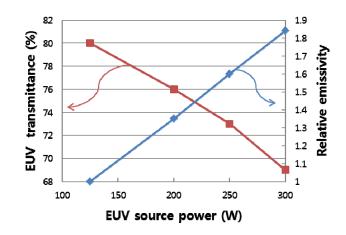


Figure 11. EUV transmittance and emissivity of an EUV pellicle against EUV source power under the condition of keeping temperature at 400°C

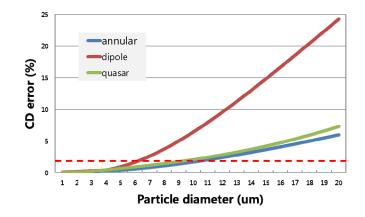


Figure 12. CD error against the size of particle in the pellicle

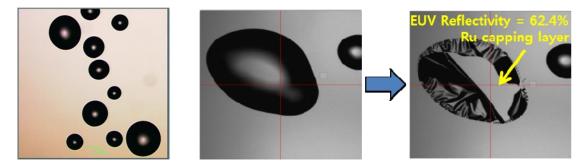


Figure 13. Bulging defect in EUV mask(a). Bulge occurred at Ru-capping layer(b).

### 4. RESIST

Figure 14 shows the Z-factor of the selected resists screened last few years, which shows continuous progress so far. Now the resist performance satisfies the requirements of developing 7nm logic, however in order to attain the productivity goal resist dose needs to be reduced further. In addition the infrastructure for resist qualification like defect and dose will be necessary before high volume production starts.

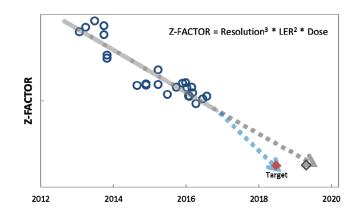


Figure 14. RLS improvement trend in EUV resist

### 5. PROCESS COMPARISON

Pattern uniformity of ArF-i multiple patterning was compared with EUV single exposure as shown in Figure 15(a). Expectedly EUV shows better uniformity in CD and also in contact resistance as a consequence.

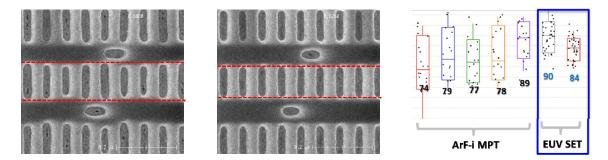


Figure 15. (a) Comparison of contact CD uniformity between ArF-i multiple patterning and EUV single exposure, (b) contact resistance

### 6. HIGH-NA EUV

Current 0.33NA would not provide enough resolution for 3nm logic and high-NA EUV will be needed in order to keep scaling down. There has been a long and elaborate investigation on high-NA optics and exposure tools. But in order to enabling high-NA, all the elements of EUV lithography need to be prepared once again in parallel with exposure tool. Table 1 shows the list of requirements. Especially resist would be most significant challenge and resist stochastic modelling was utilized to estimate the performance gap between current resist and the one for high-NA.

Lithography (S-Litho) tool was used for this purpose and hundreds of SEM images for the one of the best CAR at different exposure conditions were used for calibrating all the parameters both for continuous and stochastic modeling<sup>5,6</sup>. Figure 16 shows the simulation results of LCDU of CH pattern against pitch. By using 0.55NA LCDU decreases from around 3.5nm to 2.5nm due to the increase of NILS. But at 32nm pitch, which is supposedly the CH pitch for 3nm logic, LCDU increases again up to 4nm, while 2.4nm is needed in order to keep LCDU of less than 15% of half pitch. Since the resist used in this modeling is characterized by low local variation and high dose, a lot of improvements will be needed in order to satisfy both variation and productivity demands. Second issue is that the depth of focus in 0.55NA will be as small as one-third of that in 0.33NA according to Rayleigh's formula. Leveling performance of exposure tool, CMP process, and wafer flatness are to be improved accordingly. In addition thin absorber should be prepared to reduce the best focus shift as well. Using anamorphic optics will result in inevitable stitching for chips bigger than half-field and specific solution would be required. Since the 0.55NA tool will be much higher and heavier, a new dedicated fab is to be built to install it. Mask infrastructure also should be prepared timely, which will need industry-wide collaboration similarly as experienced in building current 0.33NA EUV infrastructure.

Table 1. Requirements for enabling high-NA EUV

- 1. Resist satisfying RLS requirement and without pattern collapse
- 2. Solution for small DOF( $\sim 1/3$  of 0.33NA)
- 3. Solution for stitching(due to half-field)
- 4. New fab construction
- 5. Mask infrastructure high-resolution blank inspection tool, pattern inspection tool, high-NA EUV-AIMS

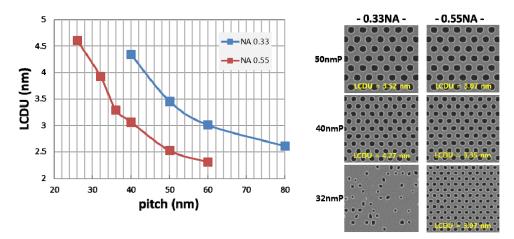


Figure 16. LCDU against CH pitch both for 0.33NA and 0.55NA(a), simulated SEM images(b)

# 7. SUMMARY

Source power, droplet generator lifetime, and blank defectivity are now approaching HVM goals. Collector lifetime is the major contributor to availability loss nowadays and a rapid improvement is needed. Scanner defectivity requires further improvement and especially all the parts should be maintained in a clean status during both fabrication and integration. Pellicle membrane of longer lifetime, and higher transmittance are needed. Current resist performance can support 7nm development but sensitivity needs to be improved to attain the productivity goal. High-NA needs to be prepared in each elements of lithography in addition to the exposure tool itself, which would require industry-wide collaboration.

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