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## InGaAs DETECTORS AND FPA'S FOR A LARGE SPAN OF APPLICATIONS: DESIGN AND MATERIAL CONSIDERATIONS

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### I. INTRODUCTION

Compared with the other Infrared detector materials, such as HgCdTe (or MCT) and lead salts (e.g.: PbS, PbSe, PbSnTe, ...), the history of InGaAs FPA's is not that old. Some 25 years ago the first linear detectors were used for space missions [1,2]. During the last 15-20 years InGaAs, grown lattice matched on InP, has become the work horse for the telecommunication industry [3] and later on for passive and active imagery in the SWIR range. For longer wavelengths than 1.7  $\mu\text{m}$ , III-V materials are in strong competition with SWIR MCT and till now the performance of MCT is better than high In-content InGaAs. During the last years some alternatives based on quaternary materials [4] and on Superlattice structures [5] are making gradual progress in such a way that they can yield performing Focal planes in the (near) future.

As the SWIR wavelengths range covers a large variety of applications, also the FPA characteristics and mainly the ROIC properties need to be adjusted to fulfil the mission requirements with the requested performance. Additionally one has to bear in mind that the nature of SWIR radiation is completely different from what is usually encountered in IR imaging. Whereas the signal of thermal imagery in the Middle Wavelength (MWIR: [3 – 5  $\mu\text{m}$ ]) or Long Wavelength (LWIR: [8 – 10  $\mu\text{m}$ ] or [8 - 12  $\mu\text{m}$ ]) band is characterized by a large DC pedestal, caused by objects at ambient temperature, and a small AC signal, due to the small temperature or emissivity variations, SWIR range imagery is characterized by a large dynamic range and almost no DC signal. In this sense the SWIR imagery is resembling more the nature of Visible and NIR imaging than that of thermal imagery.

### II. SWIR APPLICATIONS

This paragraph does not pretend to be complete; but we will try to give a broad overview of possible SWIR imaging applications, based on photon flux (Table 1). Depending on the Photon flux, the authors are giving a suggestion, which ROIC to use for applications, based on that photon flux.

Table 1: Overview of SWIR applications, the associated issues with the FPA or Camera, the FPA operating mode and the ROIC configuration.

Photon Flux ( $\Phi$ ) Integration time	Application area	Problem area	Operating mode Suggested ROIC
$\Phi \leq 1$ phot/pix/sec Tint > 1 sec	<ul style="list-style-type: none"> <li>Electro-luminescence</li> <li>Raman</li> <li>Astronomy</li> </ul>	<ul style="list-style-type: none"> <li>Electro-luminescence of ROIC</li> <li>Thermal signal from Planck's tail</li> </ul>	Cooled operation LN2 – TE-3 SFD
$\Phi$ [10 – 1000] Tint [0.1 – 1 sec]	<ul style="list-style-type: none"> <li>Spectroscopy of faint sources</li> </ul>	<ul style="list-style-type: none"> <li>Dark signal non-uniformity</li> </ul>	Cooled operation TE-1 or TE-2 CTIA
$\Phi$ [800 – 40 000] Tint [20 – 100 msec]	<ul style="list-style-type: none"> <li>Night vision</li> <li>Spectroscopy</li> </ul>	<ul style="list-style-type: none"> <li>Dark signal non-uniformity</li> <li>Auto-Zero</li> <li>Noise</li> <li>Blooming</li> </ul>	Uncooled, battery operated CTIA
$\Phi$ [80.10 <sup>3</sup> - 80.10 <sup>6</sup> ] Tint [1 – 100 msec]	<ul style="list-style-type: none"> <li>regular imaging day time or artificial light</li> <li>Spectroscopy</li> </ul>	<ul style="list-style-type: none"> <li>Large dynamic range</li> <li>Image compression</li> <li>Blooming</li> </ul>	Uncooled, CTIA
$\Phi$ [20.10 <sup>6</sup> - 800.10 <sup>6</sup> ] Tint [0.1 – 1 msec]	<ul style="list-style-type: none"> <li>Hyperspectral imaging</li> <li>Long range gated</li> </ul>	<ul style="list-style-type: none"> <li>Frame rate</li> <li>Line and frame dead times</li> </ul>	Uncooled CTIA
$\Phi$ [100.10 <sup>6</sup> - 100.10 <sup>9</sup> ] Tint [10 – 900 $\mu\text{sec}$ ]	<ul style="list-style-type: none"> <li>FTIR</li> </ul>	<ul style="list-style-type: none"> <li>Charge storage</li> <li>Frame rate</li> <li>Line and frame dead times</li> </ul>	Uncooled CTIA – (B)DI
$\Phi$ [20.10 <sup>6</sup> - 4.10 <sup>12</sup> ] Tint [10 – 500 nsec]	<ul style="list-style-type: none"> <li>Gated imaging</li> <li>3D ranging</li> <li>Fluorescence</li> </ul>	<ul style="list-style-type: none"> <li>Power dissipation</li> </ul>	Uncooled CTIA - SFD

As can be seen the photon fluxes per pixel for the different SWIR applications cover more than 12 orders of magnitude. Quite often within 1 ROIC design it is possible to cover 5 to 6 orders of magnitude:

- 1 or 2 orders by different gain settings
- 4 to 5 orders with change of integration times and ROIC timing.

Consequently different FPA solutions need to be designed to cover the full range.

For most mainstream applications a CTIA configuration (see next paragraph) is the ideal detector interface: it combines image speed with linearity and a large span of possible gain settings (mainly limited by the specific capacitance of the ROIC technology node). This is very important for low noise applications as the InGaAs technology – just as most other Infrared technologies – only allows for PIN photodiodes and not for low noise fully depleted pinned diodes.

Also the requirements for certain applications are pushing the ROIC architecture to a certain solution: e.g. in an electro-luminescence application it is very important that the ROIC itself does not generate electro-luminescent signals and hence does not illuminate its own detector array. For the short integration times, the problem is the increased power dissipation in the CTIA stage in order to cope with the fast switching times and hence the evacuation of the power from the FPA.

### III. FPA ARCHITECTURE – ROIC SELECTION

#### A. FPA Architecture

A SWIR FPA consists always of a Photodiode array or PDA manufactured in InGaAs, Ge or HgCdTe which is backside illuminated and flip-chipped onto a Silicon readout circuit or ROIC. The interconnection between both dies is made via Indium solder bumps.

For SWIR imaging applications  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ , grown lattice matched on InP [6] is the preferred material scheme. After the deposition of an antireflective coating on the backside of the wafer, the detector material can be used ‘as is’, whereas for the Ge detectors the substrate needs to be thinned down to make the detector sensitive. HgCdTe manufacturers are not yet in a position to make room temperature operated photodiodes with a cut-off  $\leq 1.85 \mu\text{m}$ . Due to the material cost, HgCdTe is mainly attractive in the far end of the SWIR band, beyond the cutoff wavelength of the lattice matched InGaAs material.

#### B. General description of IR detector interfaces

For the interfacing of infrared detectors, three different archetypical circuits are used for the collection and integration of the photodetector current (see Figure 1), in the following list the circuits are listed in order of complexity:

- A Source Follower per Detector or SFD circuit, where the detector current is integrated on the photodiode itself,
- A Direct injection stage or DI, where the bias over the detector is kept low and constant independent of voltage swing on the integrating node.
- A Charge sensitive TransImpedance Amplifier or CTIA, where the bias over the detector is kept constant by an active amplifier and where the photocurrent is accumulated on the feedback capacitor.

Although being of great simplicity and often used in visible CMOS imagers (where the circuit is referred to as a “3T” cell), the SFD solution is not very attractive in IR applications, as due to the high, initial reverse bias, the dark current is high – certainly at elevated operating temperatures. The charge to voltage conversion is happening on the photodiode itself; in Si imagers the photodiode capacitance can be kept low, due to the size of the photodetector, the (low) doping and the used of pinning technology. In SWIR applications the sensitivity of the SFD structure is lower due to the high intrinsic detector capacitance in the InGaAs photodetectors [8 – 10], the size of the photodiode and the lack of fully depletion options in the regular planar InGaAs diode.

The Direct Injection (DI) structure is also a very simple and power lean interface; in its most simple approach, it requires only one integrating capacitor and 2 transistors more than the pure SFD stage. When one compares synchronous shutter solutions, the transistor and capacitor count is almost equal, as an additional Sample&Hold (S&H) stage is needed with the SFD solution. In the DI circuit the bias over the detector is kept nearly constant by the source follower transistor connected to the detector; as the detector currents are normally very small this transistor operates in the sub-threshold region and the bias variation is only 35 to 50 mV around room temperature and even considerably less at cryogenic temperatures. The DI stage works very well in thermal infrared applications where the acquired signal is characterized by a high DC signal pedestal and low contrast ratio.

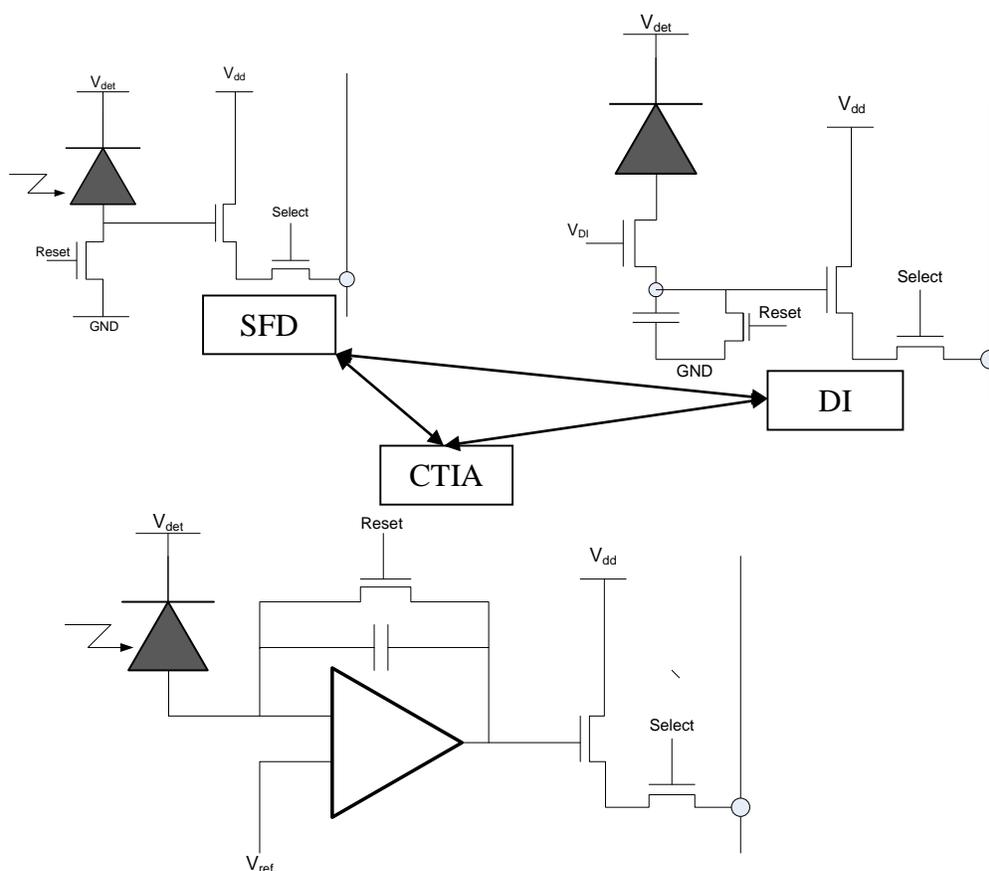


Figure 1: The 3 basic interfacing circuits for Infrared detectors:

- SFD: Source follower per detector, Charges are accumulated on detector capacitance
- DI: Direct Injection stage, detector is kept at constant bias
- CTIA: Charge sensitive TransImpedance Amplifier

On the other hand the SWIR InGaAs detectors are facing a near zero DC signal and a very high contrast ratio of the signal. Under very low light level conditions the DI stage suffers from a considerable image lag, as can be derived from the injection efficiency formula (1): [10,11]

$$\eta_{inj} = \frac{G_m \cdot R_{det}}{1 + G_m \cdot R_{det}} * \frac{1}{1 + \frac{j\omega C_{Det} \cdot R_{det}}{1 + G_m \cdot R_{det}}} \quad (1)$$

With  $R_{det} = \frac{dV_{det}}{dI_{det}}$

And  $G_m = \frac{dI_{det}}{dV_{gs}} \approx \frac{I_{det}}{nkT/q}$ , with n: 1... 2.

In a Buffered DI stage (BDI), the image lag can be reduced by 1 to 3 orders of magnitude depending on the open loop gain of the amplifier in the feedback loop. But quite often the dynamic range of a SWIR imager is  $10^4$ , resulting in lag effects at the real dark parts of the image. By the introduction of the feedback amplifier, the BDI loses part of its attractiveness wrt to the next stage, the CTIA.

### C. CTIA for regular SWIR detector interfacing

As a result, the only low dark current, low lag and broad application interface circuit for SWIR detectors is the CTIA interface stage; despite of its transistor count and of the higher unit cell power dissipation. [12-14] The last argument can be easily overcome by making the power dissipation in the interface stage variable and controlled by an on-board DAC. For high sensitivity applications, where a small integration capacitor is required the transistor count is also not really an issue. In any case the CTIA interface yields a linear, low lag interface for SWIR detectors, capable of spanning an integration time range from 100 nsec up to 1 sec or longer, depending on the cooling of the detector (see also Table 1).

### D. Low light level SWIR detector interfacing

When one analyses more carefully the applications, requiring very long or very short integration times (see also Table 1), the CTIA is operating at its limits. Due to the presence of continuously active transistors, the detector interface generates itself electro-luminescence photons, even when the CTIA is operated in deep sub-threshold regime. This photon flux is contributing to the dark signal of the detector; even when the detector is shielded from the silicon of the ROIC. The generated light is wave-guided in the substrate and tends to escape from the sides of the chip. For those applications the integration time is very long and hence the detectors need to be cooled to 200 K or even 77K; under these assumptions, the detector shunt resistance becomes very high and hence the SFD stage seems to be the best alternative, such as demonstrated by the Virgo [9], Hawaii [15] and Cougar device [16]. In this interface circuit only one detector interface is active at the time instead of all matrix elements in parallel. For slow scan applications this SFD buffer transistor can drive the output load capacitance or it can be assisted by one properly shielded current amplifier stage. Although the SFD for IR detectors has a low conversion gain, good Signal to Noise Ratios (SNR) can be obtained by optimizing the bandwidths of the circuit and by implementing Correlated Double Sampling (CDS) or Fowler sampling.

### E. High flux SWIR detector interfacing

If we look to the opposite range of photon fluxes and integration times, the CTIA needs to sink more and more current, to drive the output load on the integration slope and to stabilize the circuit in shorter delays. Under these circumstances the matrix of detector interfaces is dissipating more and more power and this power consumption needs to be multiplied with the number of pixels. For this reason low power consumption schemes are again entering under the attention. For FTIR applications the average DC level of the signal is set at app. 50 % of Full Well (FW) and the modulation of the signal is seldom larger than 30% FW. Under these conditions a carefully designed DI stage can result in a good SNR ( $\geq 80$  dB) with a minimal power consumption.

Also for short Tint time of Flight applications a SFD can result in reasonable performance with minimal power dissipation. The amount of electrons returning from a distant source is  $< 100 e^-$  and there is no time for waiting for the CTIA stabilization. An SFD stage with a dual S&H can deliver the signals for a CDS operation. The S&H operation is executed in charge domain, where the partitioning noise is low with a careful design of the switches. Quite often the pulse repetition rate is low, resulting in a small bandwidth for the CDS operation at this stage the signal is also amplified before putting it on the output bus.

## IV. DETECTOR MATERIAL SCHEMES

As indicated in the introduction, the SWIR InGaAs was initially developed for telecommunications; high quality layers and diodes, grown lattice matched on InP substrates (see Figure 2 – orange ellipse) were developed, later on these diodes were grouped in order to form linear arrays and FPA's. When properly grown, originally with LPE, but now almost exclusively with MOCVD, the dislocation density is low and the dark current of the photodiodes is comparable with Si diodes taking into account the bandgap scaling rules.

But when one deviates from the "golden"  $\text{In}_{0.47}\text{Ga}_{0.53}\text{As}$  composition, the lattice constant of the ternary compound changes rapidly and the material degrades quickly with the deviating lattice constant. Other binary substrates, such as GaAs and InAs are having too much deviating lattice constants to yield high quality detectors. Several attempts have been made to grown extended InGaAs compositions on a thick lattice matching buffer layer, but still the shunt resistance is not good enough for 2D FPA quality. For linear arrays the material is good enough as the detector interface on the ROIC can be complex enough to cope with the low detector shunt resistance. In longer wavelength QWIP devices the GaAs/InGaAs system is quite often used with good quality and good performance. The difference with plain PIN structures is here that the QWIP layers are thin enough ( $< 5$  nm), so that they can be kept under strain without relaxation by dislocations.

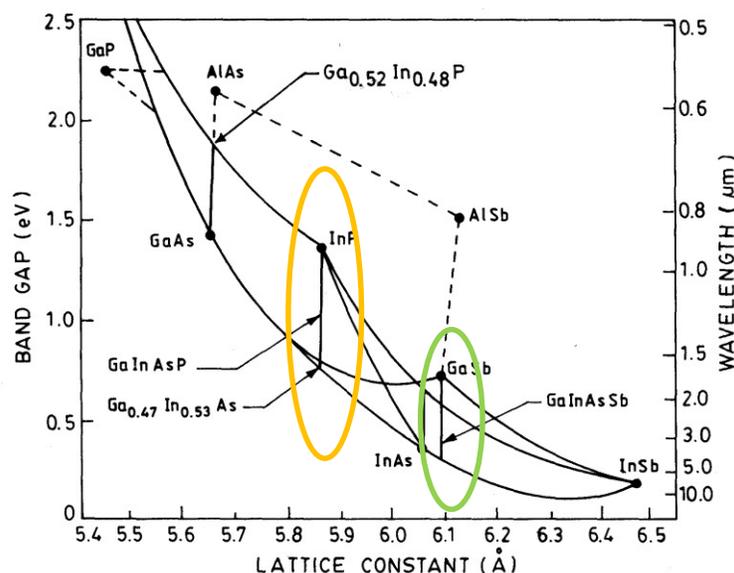


Figure 2: Bandgap diagram of III-V compounds vs lattice constant. Picture courtesy of D.N. Bose [17]

During the last years and under the influence of the Type 2 Superlattice (T2SL) detectors, a lot of attention is paid to the quaternary InGaAsSb scheme, grown on GaSb (see Figure 2 – Green ellipse). In this case the bandgap can be changed over a large range without losing in material quality [18]. The growth technique is complemented by the use of an Interfacial Misfit Array (IMA), which makes it possible to make under controlled conditions an abrupt change of the lattice constant between e.g GaAs and GaSb, while maintaining simultaneous good material quality.

Under these conditions and by applying the proper passivation layer, it is possible to fabricate InGaAsSb photodiodes which have almost the same shunt resistance as comparable MCT diodes. Presently actions are taken to upscale the technology from single photodiodes to linear and 2D photodiode arrays.

## V. CONCLUSIONS

III-V detectors exist only for some 27 years. Since their invention in 1977 by Pearsall, InGaAs photodiodes have made big progress and nowadays Megapixel FPA's are in production with several suppliers. At this moment InGaAs, grown lattice matched on InP is the only room temperature operated SWIR detector with a cut-off of 1.7  $\mu\text{m}$ . For longer wavelengths MCT was long time more mature, but recent developments with GaSb based detectors show almost equal performance under the same operational conditions.

The different SWIR applications span an incredible 12 order of magnitude photon flux and typical integration times range from tens of nanoseconds to minutes. For a broad range of photon fluxes CTIA stages are the ideal detector interface for SWIR detectors, as they yield excellent linearity, low lag and a broad range of charge to voltage conversion factors. Only for the extreme limits of the photon flux, other interface stages – mainly SFD – are more favourable. For ultra low-light application, a carefully designed SFD stage generates a negligible electroluminescence signal. For very short integration times the same SFD stage has only very short transition effects, resulting in a better and lower noise signal.

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