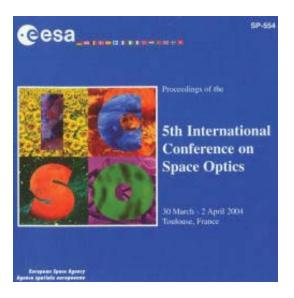
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DEVELOPMENT OF A 750x750 PIXELS CMOS IMAGER SENSOR FOR TRACKING APPLICATIONS

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ABSTRACT

Solid-state optical sensors are now commonly used in space applications (navigation cameras, astronomy imagers, tracking sensors...). Although the chargecoupled devices are still widely used, the CMOS image sensor (CIS), which performances are continuously improving, is a strong challenger for Guidance, Navigation and Control (GNC) systems. This paper describes a 750x750 pixels CMOS image sensor that has been specially designed and developed for star tracker and tracking sensor applications. Such detector, that is featuring smart architecture enabling very simple and powerful operations, is built using the AMIS 0.5µm CMOS technology. It contains 750x750 rectangular pixels with 20µm pitch. The geometry of the pixel sensitive zone is optimized for applications based on centroiding measurements. The main feature of this device is the on-chip control and timing function that makes the device operation easier by drastically reducing the number of clocks to be applied. This powerful function allows the user to operate the sensor with high flexibility: measurement of dark level from masked lines, direct access to the windows of interest... A temperature probe is also integrated within the CMOS chip allowing a very precise measurement through the video stream. A complete electro-optical characterization of the sensor has been performed. The major parameters have been evaluated: dark current and its uniformity, read-out noise, conversion gain, Fixed Pattern Noise, Photo Response Non Uniformity, quantum efficiency, Modulation Transfer Function, intra-pixel scanning. The characterization tests are

detailed in the paper. Co⁶⁰ and protons irradiation tests have been also carried out on the image sensor and the results are presented. The specific features of the 750x750 image sensor such as low power CMOS design (3.3V, power consumption<100mW), natural windowing (that allows efficient and robust tracking algorithms), simple proximity electronics (because of the on-chip control and timing function) enabling a high flexibility architecture, make this imager a good candidate for high performance tracking applications.

1. INTRODUCTION

CMOS Image Sensors (CIS) are recognized since more than ten years as the potential successor to CCDs for Guidance, Navigation and Control (GNC) applications (see for instance [1] to [4]). Indeed, CIS feature several functional and operational advantages making these devices natural candidates for these types of space applications: direct access to windows of interest, onchip control and processing electronics, low power consumption, better radiation tolerance... In addition, modern CIS designed using standard CMOS processes feature electro-optical performances equivalent to those of standard front-illuminated CCDs, and even improved performances can be expected in the short term with the emergence of specific designs and technologies [5].

In the framework of their development of CIS for space applications, EADS-Astrium and Supaéro-CIMI have built in 1997 a first 512x512 pixels array devoted to GNC applications, featuring very good electro-optical performances [6]. Thanks to this success, and in the frame of the development of a miniature star sensor (SSM contract awarded by CNES in 1999), a specific device was designed to fit the SSM requirements [7], [8]. Fig. 1 presents a mock-up of this miniature star sensor. This paper presents the main results from the extensive characterisation of the CIS as designed and built for the SSM.



Fig. 1: mock-up of the miniature star sensor developped by EADS-Astrium under CNES contract

2. DEVICE DESCRIPTION

The CIS dedicated to the miniature star tracker is built using AMIS 0.5µm CMOS technology. General overview of the device is depicted in Fig. 2 and Fig. 3 shows the device in its package.

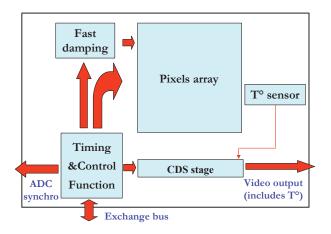


Fig. 2: general overview of the CIS dedicated to the miniature star sensor

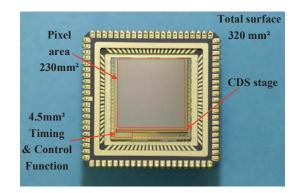


Fig.3: the CIS device in its package for characterisation

The CIS device features 750x750 rectangular pixels with 20µm pitch. The geometrical pixel fill factor is high (around 60%) with a topology of the sensitive zone optimised for applications based on centroiding measurements. The pixel circuitry is based on a photogate topology in order to allow real correlated double sampling processing (and thereby lower temporal noise). Only one output stage is implemented which is sufficient for most of the sensor applications. The charge to voltage conversion factor has been designed to be equal to $10\mu V/e$ -, which is a compromise between temporal noise (in e-) and dynamic range. Masked lines are implemented to track the dark current variation and to measure the column fixed pattern noise (FPN). The video output is on-chip sampled, using CDS stages, cancelling pixel FPN and kTC plus low frequency noises and significantly relaxing the external video chain design compared to CCDs. An outstanding feature of this device is its on-chip control and timing function. From simple master clock and control bus, this function operates the image sensor and generates synchronization signals for the processing of the analogue output signal (digitization...). The on-chip control and timing function makes the device operation easier by drastically reducing the number of clocks to be applied. Several read-out modes are available: (i) autonomous continuous mode; (ii) variable integration time mode; (iii) fast total flush; (iv) multiple read-out mode; (v) dynamic windowing mode, which is the most useful one for tracking applications. In this latter mode, the number, location and size of multiple sub-windows that can be acquired can be modified at frame rate (Fig. 4). It should be noticed that the acquisition of overlapping sub-windows is possible.

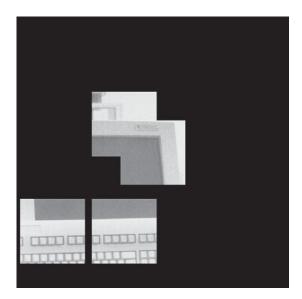


Fig.4: example of dynamic windowing mode as offered by the CIS device

A temperature probe is integrated within the CMOS chip. When compared to external probes mounted in the package, this leads to more accurate measurement as it is measured on the die itself. As the probe information is read-out via the video link, this function does not require any specific interface.

Low power consumption is one of the major advantages of CMOS image sensors when compared to CCDs. This is particularly the case when considering the power requested for the total imaging function thanks to the low number of peripheral chips required for the CMOS device operation (no clock drivers, simplified video chains...). The measured power consumption of the array is less than 80 mW. More information about the device operation is available in [9].

3. ELECTRO-OPTICAL CHARACTERIZATION

In order to minimize the development risk of the device, and in view of testing various pixel designs with respect to radiation behaviour, a test vehicle, shown on fig. 5, was built in the frame of the SSM program. This device was characterised and tested against radiations (latch-up and total dose: [8]), allowing the best pixel type to be selected.

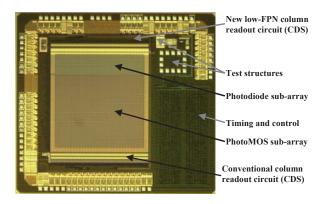


Fig. 5: a test vehicle was built to secure the development of the SSM CIS device

Electro-optical characterisation of the 750x750 pixels array was performed for operating conditions as close as possible to those of the SSM application. The clock diagram used was the nominal one as defined by the design of the array. The read-out frequency was set equal to 670 kHz, which is that of the SSM. For each measurement, the temperature could be adjusted. A platinum probe was glued onto the device package and tracked in real time in order to provide absolute calibration of the on-chip temperature probe. Except for the temporal noise measurements (and conversion factor determination), the data were averaged over 100 frames. Four test bench configurations were used: darkness conditions with variable temperature, uniform illumination, spot scan illumination and MTF measurements. Table 6 summarizes the main figures as obtained from the device characterization. Some specific performances are discussed in the following.

Table 6: main electro-optical parameters			
of the SSM CIS device			

Parameter	Associated figure
Conversion factor	9.2 μV/e-
Linear dynamic range	58 ke-
Temporal read-out noise	32 e- rms
FPN (15x15 pixels windows)	3.5 mV (1 σ)
Dark current @ 20°C	600 pA/cm ²
DSNU (15x15 pixels windows)	10% (1 σ).
Peak detection efficiency	28% @ 610 nm
PRNU (15x15 pixels windows)	$<0.7\%$ (1 σ) @ 650 nm
MTF @ Nyquist frequency	X=0.46/Y=0.54 @ 500nm X=0.31/Y=0.40 @ 650nm X=0.28/Y=0.35 @ 800nm

A topic which is not often investigated for CMOS sensors is their ability to deal with a low amount of charges (weak stars in a star tracker for instance). Fig. 7 shows the lowest part of the linearity characteristics, demonstrating the ability of the device to manage few 10s of electrons.

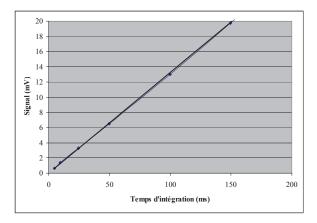


Fig. 7: demonstration of the good linear behaviour of the device even for low amount of signal

Dark current was characterised versus temperature over the 0 to 25°C range. The activation energy is equal to 0.16 eV and the dark current doubles each 8.2°C. Fig. 8 presents the dark current spatial map, showing a flat distribution except along a 50 rows external ring, corresponding to the ball effect already observed for other CMOS devices.

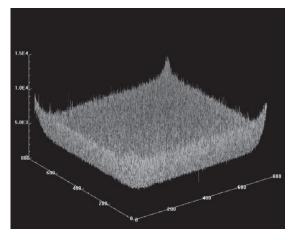


Fig. 8: dark current spatial cartography of the SSM CIS device

Fig. 9 presents the same type of map for the responsivity of the array under uniform illumination (650 nm), showing a nearly flat behaviour and a very low number of defective pixels. It should be noticed that 60% of the devices from the foundry do not feature any major cosmetic defect (dead line or column).

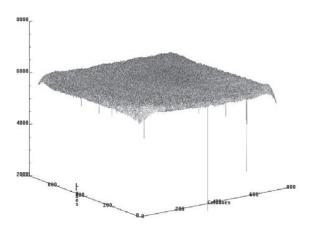


Fig. 9: responsivity spatial cartography of the SSM CIS device for 650 nm uniform illumination

Fig. 10 and Fig. 11 present respectively the along line and along column intra-pixel sensitivities, which were characterised using the spot scan method (spot diameter around 4 μ m and 450 nm illumination). The intra-pixel spatial response is very uniform, which is an important point for applications based on centroiding processing.

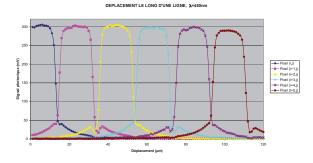


Fig. 10: along line intra-pixel sensitivity (450 nm spot scan)

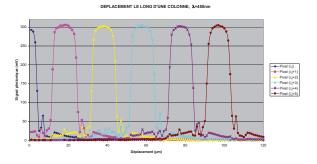


Fig. 11: along column intra-pixel sensitivity (450 nm spot scan)

As presented in Table 6, the MTF is better along the Yaxis with respect to the X-axis. This is mainly due to the rectangular shape of the in pixel photosensitive area. MTF degrades when the wavelength increases. Indeed, longer wavelength photons penetrate deeper in the silicon volume and can be diffusion collected by neighbouring pixels instead of being directly collected by the illuminated pixel. CMOS processes optimised for imaging applications [5] are expected to strongly reduce this effect.

4. BEHAVIOUR AGAINST IRRADIATIONS

It should first be noticed that the CMOS imaging array developed for the SSM application was not designed in view of being radiation tolerant, as the specification for this application is not too much harsh. SSM devices Co⁶⁰ irradiated using were source at DESP/CERTONERA facility (Toulouse) and highenergy protons beam (from 59 to 100 MeV) at Centre de Protonthérapie (Orsay) thanks to the use of CNES beam time. No latch-up tests were performed for this device as a test vehicle built with the same technology had been tested against heavy ions by CNES at the IPN Orsay facilities [8]. For this device, no latch-up sensitivity was observed up to 58.2 MeV (mg/cm²).

4.1 Ionising radiation campaign

The Co⁶⁰ tests of the SSM array confirmed and refined the results as observed during the test vehicle ionising radiation campaign [8]. Three levels of dose were tested: 5, 10 and 15 krad(Si), the SSM specification being 10 krad(Si). The dose rate was equal to 150 rad(Si)/h. Measurements were performed few days after irradiation. Then, 100°C/168 hours baking was performed and the devices were characterised again. Some parameters appeared to be as insensitive to the effect of the ionising radiation, at least up to 15 krad(Si) : dynamic range, conversion factor, read-out noise and column FPN, as presented in table 12 which summarizes the main results.

Table 12: electro-optical degradation after 10 krad(Si) ionising irradiation and 100°C/168 hours baking (EOL) compared to results before irradiation (BOL).

Parameter	BOL	EOL
Dynamic	55-60 ke-	55-60 ke-
Conversion factor	$\approx 9 \ \mu V/e$ -	$\approx 9 \ \mu V/e$ -
Read-out noise	30-35 e- rms	30-35 e- rms
HF FPN	3.5 mV (1 σ)	3.5 mV (1 σ)
Dark current@25°C	850pA/cm ²	4000pA/cm ²
HF DSNU	10% (1 σ)	4% (1 σ)
Detection efficiency	26% @650 nm	24% @650 nm
HF PRNU@650nm	0.6 % (1 σ)	<1.5 % (1 σ)

Fig. 13 presents the dark current degradation versus ionising radiation dose before and after the baking operation, showing a reverse annealing effect. Fig. 14 shows that, on the other hand, the relative DSNU (Dark Signal Non Uniformity) decreased versus total dose.

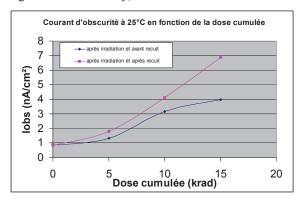
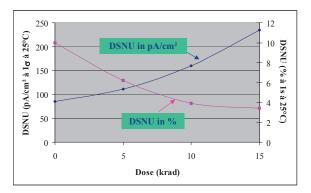


Fig 13: evolution of dark current versus ionising radiation before and after 100°C/168 hours baking



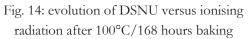
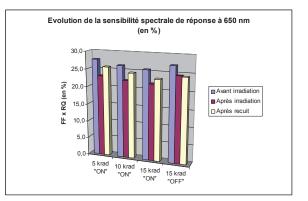
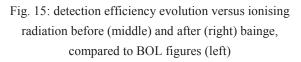


Fig. 15 presents the evolution of detection efficiency versus ionising radiation before and after 100°C/168 hours baking, with respect to pre-irradiation figures.

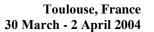
Based on the ionising radiation campaign results, the SSM CIS device behaviour is close to what was expected from the test vehicle radiation results and the degradation of the electro-optical performances are low enough to be acceptable for the SSM application. One of the most interesting result is the dark current reverse annealing behaviour which can be observed after baking operation.





4.2 Protons campaign

The devices were irradiated for three "energy/fluence" combinations calculated to provide the same degradation if the NIEL model could be applied, $2.1.10^{10}$. $2.4.10^{10}$ $2.75.10^{10}$ and respectively protons/cm² corresponding to 59, 80 and 100 MeV. The equivalent total dose was in the 2.5-3 krads(Si) range for these three conditions. Based on results published by other teams ([10], [11], [12]), the main expected effects should have been due to displacement effects (as for CCD devices), i.e. degradation of the DSNU, of the detection efficiency and of the low frequency temporal noise (Random Telegraph Signal (RTS) noise). Based on the actual post-irradiation characterisation results, only the CIS dark current slightly increases for nearly all the pixels, presumably due to the ionising effect. As shown on the cumulative histogram presented in Fig. 16, dark currrent at 28°C increases by more than 400 pA/cm² for 5% of the pixels and by more than 1.6 nA/cm² for 1% of the pixels.



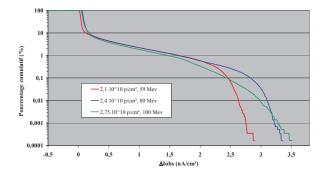
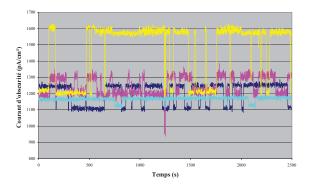
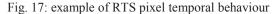


Fig. 16: cumulative histogram of dark current at 28°C for the 3 "energy/fluence" combinations

Approximately 4% of the irradiated pixels featured RTS behaviour with amplitude in the 50-400 pA/cm² range and with period in the few sec to 10 mn range when observed at ambient temperature. Fig. 17 presents a typical behaviour of few pixels.





Based of the analysis performed by CNES experts, it is suspected that the NIEL model is not the only one to be involved in the device degradation. Other causes seem to be implied, which explains that the observed degradations differ from each other according to the actual "energy/fluence" combination.

5 CONCLUSIONS

A 750X750 pixels CMOS image array was developed for the SSM miniature star sensor application, featuring functionalities dedicated to tracking applications. The electro-optical characterisation demonstrated that the associated performances are very good and can fulfil the SSM requirements. The degradations induced by ionising radiations showed to be acceptable with respect to the SSM specifications. As expected, dark current and low frequency noise were degraded by protons irradiations for few pixels. Such an impact can be managed for the SSM application as these few pixels can be discarded during the data processing.

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REFERENCES

[1] Fossum E. et al. Application of the active pixel sensor concept to guidance and navigation, *SPIE proceedings*, Vol. 1949, 256-264, 1993

[2] Clark C. C. et al. Application of new technology to future celestial trackers, *SPIE Proceedings*, Vol. 2466, 100-107, 1995

[3] Salomon P. et al. Active pixel sensors for autonomous spacecraft applications, *SPIE proceedings*, Vol. 2810, 166-175, 1996

[4] Lelong P. et al. Miniature GNC sensors using APS devices, *ESA Proceedings about 4th ESA International Conference on Spacecraft Guidance, Navigation and Control Systems*, 1999

[5] Saint-Pé O. et al. research grade CMOS image sensors for demanding space applications, *this proceeding*

[6] Saint-Pé O. et al. Development and characterization of active pixel sensors for space applications, *SPIE proceedings*, Vol. 3440, 24-36, 1998

[7] Saint-Pé O. et al. High performance monolithic CMOS detectors for space applications, *SPIE proceedings*, Vol. 4540, 318-327, 2001

[8] Larnaudie F. et al. Development of highperformance monolithic CMOS detectors for space applications, *SPIE proceedings*, Vol. 4823, 222-232, 2002

[9] APS750 CMOS Image Sensor datasheet, October 2003

[10] Bogaerts J. et al. Random Telegraph Signals in a radiation-hardened CMOS Active Pixel Sensor, *IEEE Trans. Nucl. Sci.*, Vol. 49, n°1, 249-257, 2002

[11]Bogaerts J et al. Total dose and displacement damage effects in a radiation-hardened CMOS APS, *IEEE Trans. Electron. Devices*, Vol. 50, n°1, 84-90, 2003

[13] Hopkinson G et al. Radiation effects on a radiation tolerant active pixel sensor, presented to the RADECS 2003 conference