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DESIGN OF A HIHGLY INTEGRATED VIDEO ACQUISITION MODULE FOR SMART VIDEO FLIGHT UNIT DEVELOPMENT

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ABSTRACT

CCD and APS devices are widely used in space missions as instrument sensors and/or in Avionics units like star detectors/trackers. Therefore, various and numerous designs of video acquisition chains have been produced.

Basically, a classical video acquisition chain is constituted of two main functional blocks: the Proximity Electronics (PEC), including detector drivers and the Analogue Processing Chain (APC) Electronics that embeds the ADC, a master sequencer and the host interface.

Nowadays, low power technologies allow to improve the integration, radiometric performances and power budget optimisation of video units and to standardize video units design and development.

To this end, ESA has initiated a development activity through a competitive process requesting the expertise of experienced actors in the field of high resolution electronics for earth observation and Scientific missions. THALES ALENIA SPACE has been granted this activity as a prime contractor through ESA contract called HIVAC that holds for Highly Integrated Video Acquisition Chain.

This Paper presents main objectives of the on going HIVAC project and focuses on the functionalities and performances offered by the usage of the under development HIVAC board for future optical instruments.

1 INTRODUCTION

1.1 ESA objectives

Compilation of optical instruments inputs from a large range of ESA missions for science & earth observation program results in ESA objective to develop on the same die and based on a commercial technology (hardened by design) :

- Front-end functions to accommodate CCD and APS detectors
- Analog-to-Digital Conversion function
- Digital Interfaces to a SpaceWire network

In order to integrate in Space Market, an European IP Design House Leader, MIPS/CHIPIDEA(Portugal) has been selected by ESA for the VASP (Video Acquisition Signal Processor) ASIC development, in the frame of the HIVAC project.

1.2 HIVAC project organisation and objectives

HIVAC project organisation is presented hereafter :

Prime :
THALES ALENIA SPACE for AIV and System Test

Sub-contractors :
MIPS/CHIPIDEA for VASP development
THALES ALENIA SPACE for HIVAC Breadboard development

Main Technical objectives of HIVAC project are:

- Develop multi video acquisition board with radiometric performances able to cope with most of ESA missions
- Develop high accuracy / medium speed Video Acquisition Signal Processing ASIC (VASP)

In order to improve integration and miniaturisation of video units and to design functional bricks allowing smart flight unit development for future missions.

1.3 HIVAC project workplan

HIVAC project is split in 2 phases (i.e. Phase 1 & Phase 2) :

Table 1 HIVAC project work plan

Phase 1 Objectives	- Specify and design (at architectural level) VASP ASIC & related HIVAC breadboard - Issue preliminary tests plans and procedures - Issue VASP & HIVAC feasibility plan
Phase 2 Objectives	- Perform the detailed design of VASP ASIC and HIVAC breadboard - Manufacture VASP prototypes & HIVAC breadboard - Test and Characterize VASP & HIVAC breadboard (electrical and radiations tests) - Issue consistent documentation ready to be used for space program evaluation

Phase 1 of HIVAC project has been closed successfully. HIVAC project phase 2 is actually on going and detailed design of VASP and HIVAC breadboard finalisation is pending.

2 HIVAC ARCHITECTURE

HIVAC architecture has been derived from a wide compilation of mission instruments and accommodates a wide range of detectors.
Consequently, HIVAC might be used easily to accommodate application as:

- § Star tracker head
- § Smart sensors
- § Science missions : Optical instruments
- § Earth Observation missions : Medium resolution optical spectrometers and high resolution imaging spectrometer
- § Video monitoring camera

HIVAC architecture merges PEC and APC on the same board within the functional block diagram shown in Fig. 1.

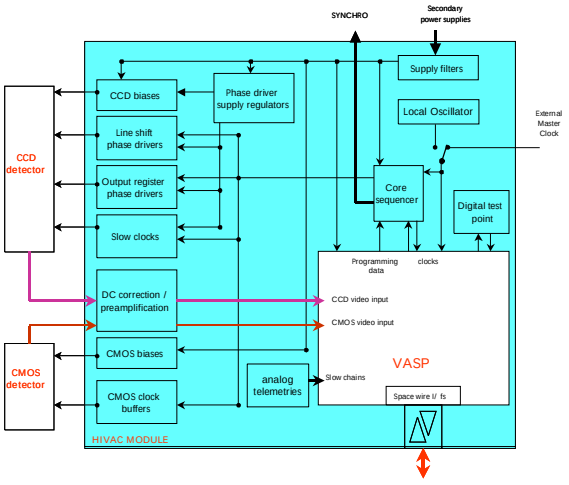

Fig. 1 : HIVAC functional block diagram

HIVAC integrates VASP ASIC for video signal processing and SpaceWire Interface. It generates sequencing for detectors and VASP from embedded local oscillator or external main master clock.

Four analog telemetries are converted from analog to digital by VASP for housekeeping control.

An optional pre-amplification / DC correction stage is available on video inputs. This stage performs DC correction (sequenced pre-clamp for CCD detector output and DC subtraction for APS/CMOS detector output), common mode noise rejection, pre-amplification (up to x16) and pseudo-differential to differential conversion to optimize SNR (Signal to Noise Ratio) and align video signal range to the VASP input range.

This pre-amplification / DC correction stage is optional, since VASP is also compatible of pseudo-differential signal allowing simple connection between focal plan assembly and VASP (only capacitors are required in case of CCD to suppress the high DC voltage at CCD output).

HIVAC is able to drive CCD detectors (clocking and biasing) or APS/CMOS detectors (clocking, biasing and serial link programming).

In the frame of the HIVAC project, two kinds of detector (CCD and CMOS) have been selected in order to characterize HIVAC in representative conditions with real detectors :

- § E2V CCD55-20 selected for Sentinel 3
- § ULIS 640x480 µbolometer candidate for infrared uncooled cameras

Consequently, HIVAC breadboard has been designed to interface with these two detectors and manage their sequencing modes and programmability accordingly .

3 VASP PRESENTATION

3.1 VASP architecture

VASP design is based on high performance analog block functions for signal conditioning and digital block functions for SpaceWire RMAP signal interfacing.

Table 2 details main VASP specifications.

VASP integrates a complete analog front-end with Analog to Digital conversion, including video input multiplexer (3 pseudo-diff or diff video inputs), correlated double sampler (CDS), programmable gain amplifier (PGA), 16-bit 3MSps analog to Digital Converter (ADC) and a full optical black on board correction/regulation algorithm.

The VASP ADC is based on a fully differential high speed low power pipeline core including on board calibration algorithm for Integral Non Linearity (INL) and Differential Non Linearity (DNL) correction.

ADC have been designed to have optimal performances at 3MSps. Moreover, for applications having Pixel frequency lower than 1MHz, multi-sampling per pixel sequencing is possible to optimize SNR by averaging.

Table 2 : VASP main specifications

Power Supply	3.3V
CCD and CMOS detector compatibility	
Pixel Frequency	0.1MHz to 3MHz
ADC resolution	16bits
Video Input Range	2V or ±2V (Diff)
INL	<± 1LSB
DNL	<± 0.5LSB
Total noise at unity gain	2LSBrms
Programmable gain	From 1 to 8
SpaceWire interface	100 Mbps (DDR mode)
Power Consumption	350mWtyp
Latch-up Immunity	>70 MeV/mg/cm2 LET
Total Irradition Dose hardness	>50krad(Si)
Package is CQFP 164	

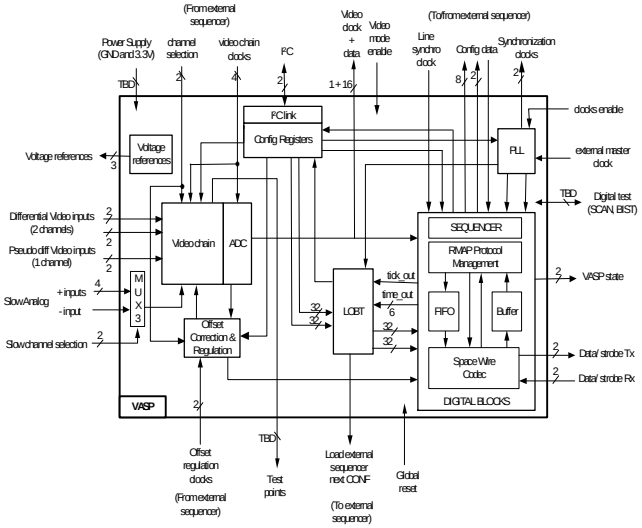

Fig. 2 : VASP synoptic

VASP Video chain uses built-in analog reference digitally programmable through SpaceWire to adjust thermal coefficient of the video chain gain.

VASP includes a Phase Locked Loop (PLL) to generate SpaceWire high frequency clock, from an external low frequency clock.

From the SpaceWire high frequency clock, it is possible to generate inside VASP two clocks for operating HIVAC core sequencer : A high frequency master clock (HIVAC system clock) and a pixel frequency. Clock characteristics are fully user programmable through SpaceWire.

VASP has four slow chain inputs for telemetries coming from HIVAC module and/or focal plan (bias voltages, current, temperature, etc).

SpaceWire RMAP (Random Memory Access Protocol) block allows video and auxiliary data packets transmission to user and allows VASP configuration. Moreover, it is possible to transmit to HIVAC core sequencer two kinds of messages directly from SpaceWire interface for HIVAC configuration through a specific 8bits parallel bus managed by VASP.

A local on board time block enables to date all events inside VASP in particular video data packets, errors, SpaceWire tick reception for user and VASP date synchronisation. It allows also to trigger configuration parameters loaded through SpaceWire accordingly to a loaded trigger date.

SpaceWire interface management inside VASP is requiring a wide part of the total power consumption (50% for digital and 50% for analog). Since applications would require stringent power dissipation specification (in particular scientific applications with very low pixel frequency), it is possible to adjust SpaceWire speeds during packet transmission and out of packet transmissions . Both speeds are adjustable independently between Fmax (100Mbps), Fmax/2, Fmax/4 and Fmin (10Mbps).

VASP integrates an I^2C interface link in a fully read/write access to VASP internal registers. This interface allows in particular to control fast VASP configuration changes (gain change at line rate, complex offset regulation loop at line rate for spectrometer application, etc).

Since digitised video flux (ADC outputs) is accessible through dedicated pins, it is possible to manage completely the VASP from the I^2C interface without using SpaceWire.

4 HIVAC CORE SEQUENCER

4.1 Functional description

HIVAC core sequencer is implemented inside a Field Programmable Gate Array (FPGA) accordingly to the following functional diagram shown Fig. 3.

HIVAC core sequencer includes 8 main functional blocks :

- The Clock generator generates from 2 external clocks provided by VASP, all the internal system clocks and Pixel period.

- The VASP parallel interface manage the reception of messages coming from VASP SpaceWire and transmitted through the dedicated 8bits bus. Two kind of messages are used for HIVAC core sequencer configurations and to update some operational parameters during HIVAC operational mode. The

message contents are distributed to each other blocks for their own configurations. VASP parallel interface is able to identify packet transmission error (use of Checksum embedded inside message) and to inform VASP of the proper reception and validation of loaded message.

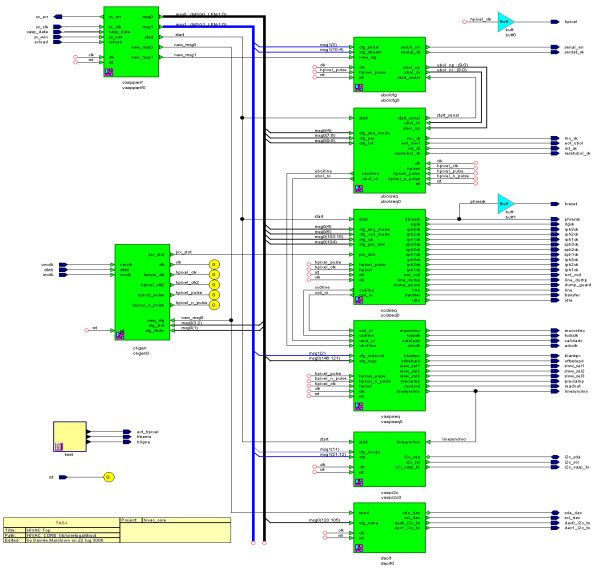

Fig. 3 : Core sequencer functional diagram

- CCD sequencer block generates CCD sequencing, accordingly to the programmed line and pixel periods and other required sequencing parameters. In particular, in the frame of the HIVAC project, CCD sequencer block has been designed to be able to manage CCD55-20 operating modes :

  - § Full frame mode : In this case, the image area of CCD is transferred into CCD store area and then all lines are moved and read in the CCD output register line.
  - § µband mode: In this case, the CCD image area is transferred into CCD store area and then detector lines are moved and dumped or read, taking into account the µband readout configuration programmed by user through VASP SpaceWire interface.

For CCD 55-20 sequencing, CCD sequencer block generates 6 image clocks, 4 register clocks and 1 slow clock (Dump Gate).

- APS/CMOS sequencer block and configuration block generate CMOS detector sequencing, accordingly to the programmed pixel period, integration time and other required sequencing or windowing parameters. In particular, in the frame of the HIVAC project, APS/CMOS sequencer block and configuration block have been designed to be able to manage 640x480 ULIS µbolometer sequencing and programming through detector serial link. All parameters loaded on Detector serial link are programmable by user through VASP SpaceWire Interface.

- Video Chain sequencer block generates all clocks required for VASP acquisition sequencing and pre-clamp sequencing (for CCD applications). In particular this block generates line synchronisation for Video data packet dating, CDS sampling times, ADC clock, optical black regulation clocks, slow chain clocks (for housekeeping), video input multiplexer clocks (in case of multi-video channels management). All generated clocks are adjustable through SpaceWire interface. For slow clocks (line rate) the adjustability step is the programmed pixel period and for fast clocks (pixel rate) the adjustability step is the internal high frequency clock generated by the clock generator (with a ratio between pixel period and high frequency clock period programmable through SpaceWire from 16 to 256).

- VASP I^2C interface manages the VASP configuration through I^2C bus. In the Frame of the HIVAC project this block has been designed to demonstrate the capability to control the VASP optical black correction registers at line rate without using the regulation loop embedded inside VASP. This functionality is essential for spectrometer applications as Sentinel 3 requiring a video offset regulation for each readout µband.

- DACs I^2C interface manages an I^2C bus allowing to program two octal DACs on HIVAC board. These DACs are used for CCD clock levels, CCD bias and µbolometer bias adjustment. DAC programming is performed using parameters loaded through SpaceWire interface.

4.2 Core sequencer selection

HIVAC core sequencer is implemented inside a FPGA. In the frame of the breadboard development Actel ProASIC PA3P1000 has been selected mainly for its on board programmability.

For Future FM units several candidate have been identified. The best candidate is the UT6325 from Aeroflex including RAM on Chip and compatible with a wide range of applications.

For applications requiring not so much programmability of detector sequencer blocks and no VASP I^2C interface block, FPGA as Actel RT54SX32/72 can be used.

5 OTHER HIVAC FUNCTIONS

5.1 Time base selection

HIVAC breadboard embeds a 9MHz local oscillator. The HIVAC sequencing can be performed using this local oscillator or using an external master clock through a SMA connector.

5.2 Power distribution

All secondary supplies are post-regulated upstream HIVAC. Only regulators and op-amp for CCD and

µbolometer interfaces are embedded on HIVAC breadboard.

All secondary supplies are filtered (Π filters) on HIVAC before being distributed to the HIVAC functions.

5.3 CCD and µbolometer Bias and clock levels setting

Adjustable regulators and/or op-amp + Ballast are used to supply CCD bias, µbolometer bias and clock drivers requiring current capability. The adjustment is performed using DACs programmed through the I^2C link managed by HIVAC core sequencer.

The Architecture of CCD and µbolometer Bias and clock level setting blocks and associated devices have been selected to reach stringent low noise specifications required by most detectors. Moreover specific filtering have been implemented to reduce noise at high frequencies.

5.4 Detector clock driving

Dedicated monolithic phase drivers are used for CCD interface. For APS/CMOS clock driving, standard CMOS logic buffer are used.

6 HIVAC OPERATING

6.1 HIVAC operating modes

The HIVAC module is able to operate in following working modes.

- **OFF**: HIVAC module is not supplied. This mode is obtained when all HIVAC input power supplies are OFF.
- **ON:** HIVAC module is supplied. This mode is obtained when HIVAC power supplies are ON. The biases at detector interface are fully operational and the detector is not sequenced. The HIVAC-VASP interface is fully operational. The HIVAC module is able to communicate with the VASP ASIC. The core sequencer is able to receive all the commands coming from the VASP. The VASP is able to be configured using SpaceWire interface.

From this ON HIVAC mode, VASP will be in NO VIDEO DATA mode for which VASP is able to be programmed through the SpaceWire interface , to communicate with the core sequencer for its configuration.

In this case, VASP is able to switch to RAMP mode and VASP CALIBRATION mode. VASP is not able to access to the OPERATIONAL mode because detector and video chain are not sequenced by HIVAC sequencer.

- **SEQUENCED:** This HIVAC mode enables detector sequencing. Analog video signals coming from detector (CCD or CMOS) are available on HIVAC interface.

From this mode, the accessible VASP modes are the same than in the previous HIVAC mode but in this case the video signal coming from detector is available at VASP input.

The VASP ASIC is able to operate in the following working modes:

- **OFF**: VASP is not supplied. This mode is obtained when all VASP input power supplies are OFF (when HIVAC is OFF).
- **NO VIDEO DATA** : VASP is supplied . All interfaces are working in a nominal way. No video data are transmitted through SpaceWire interface.
- **OPERATIONAL**: VASP is supplied. All interfaces are working in a nominal way. Video data are transmitted through SpaceWire.
- **RAMP** : VASP is supplied and a digital template is transmitted through SpaceWire instead of video data coming from video chain.
- **CALIBRATION** : VASP is supplied. SpaceWire is operating in a nominal way. The calibration of the 16-bit pipelined ADC is performed. No video data are available on SpaceWire outputs.

The links between HIVAC and VASP modes are illustrated by Fig. 4.

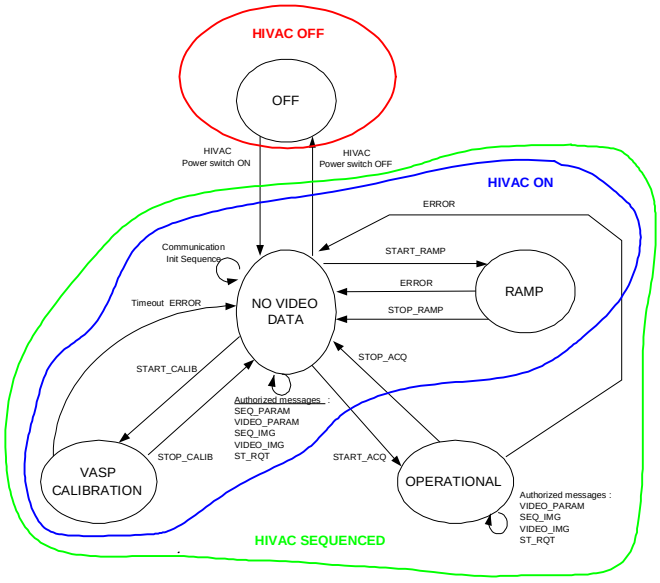

Fig. 4 : HIVAC and VASP modes

24 RMAP messages have been defined for VASP communication (cf. Table 3) with User through SpaceWire network. Since HIVAC SpaceWire

interface is integrated inside VASP, message definition are frozen except for SEQ_PARAM and SEQ_IMG messages whose final user is HIVAC core sequencer. For both messages , the content is application dependant and can be defined for future units during HIVAC core sequencer development (VASP has been defined to be independent and transparent regarding the content and the length of SEQ_PARAM and SEQ_IMG messages) .

Table 3 : HIVAC SpaceWire messages

N°	Message	Description	from	to	RMAP message type
1	ACK_CMD	Acknowledge of any user command message (START_RAMP, STOP_RAMP, START_AUX_HK, STOP_AUX_HK, START_SEQ, STOP_SEQ, START_ACQ, STOP_ACQ, START_CALIB, STOP_CALIB, ST_RQT)	VASP	User	READ_REPLY logical
2	ACK_SET	Acknowledge of any user setting message (SEQ_PARAM, VIDEO_PARAM, VIDEO_IMG, SEQ_IMG, RESET_LOBT)	VASP	User	WRITE REPLY logical
3	START_RAMP	Activate RAMP mode from NODATA mode	User	VASP	READ logical
4	STOP_RAMP	stop RAMP mode and switch VASP into NODATA mode	User	VASP	READ logical
5	RAMP_DATA	Send RAMP data	VASP	User	READ REPLY logical
6	SEQ_PARAM	Define detector sequencer parameters	User	VASP	WRITE logical
7	VIDEO_PARAM	define video chain configuration parameters	User	VASP	WRITE logical
8	START_AUX_HK	Start distribution of auxiliary and house keeping data in NODATA mode	User	VASP	READ logical
9	STOP_AUX_HK	Stop distribution of auxiliary and house keeping data in NODATA mode	User	VASP	READ logical
10	START_SEQ	Start sequencing and switch sequencer into sequenced mode	User	VASP	READ logical
11	STOP_SEQ	Stop sequencing and switch sequencer into ON mode	User	VASP	READ logical
12	START_ACQ	Start image data acquisition in NODATA mode, switch into OPERATIONAL mode and distribes pixel, auxiliary and house-keeping data	User	VASP	READ logical
13	STOP_ACQ	Stop image data acquisition and pixel, auxiliary and house-keeping data distribution in OPERATIONAL mode and switch to NODATA mode	User	VASP	READ logical
14	IMG_DATA	Send Image data with timing data on one image line basis in OPERATIONAL mode	VASP	User	WRITE logical
15	IAD_DATA	Send auxiliary data with timing data on one image line basis in NODATA or OPERATIONAL mode	VASP	User	WRITE logical
16	HK_DATA	Send house-keeping data with timing data on one image line basis in NODATA or OPERATIONAL mode	VASP	User	WRITE logical
17	VIDEO_IMG	Set video chain imaging parameters during NODATA or OPERATIONAL modes	User	VASP	WRITE logical
18	SEQ_IMG	Set sequencer imaging parameters during NODATA or OPERATIONAL modes	User	VASP	WRITE logical
19	START_CALIB	Activate CALIBRATION mode	User	VASP	READ logical
20	STOP_CALIB	Stop CALIBRATION mode and switch into NODATA mode	User	VASP	READ logical
21	ERROR	send error message in all mode after having received at least one message from user	VASP	User	WRITE logical
22	ST_RQT	Ask VASP to provide global configuration status	User	VASP	READ logical
23	ST_RPT	Provide global status	VASP	User	READ REPLY logical
24	RESET_LOBT	Reset LOBT	User	VASP	WRITE logical

7 SYNTHESIS OF PROGRAMMABILITY / VERSATILITY

HIVAC and VASP have been designed in order to accommodate a wide range of application. Therefore a large programmability and flexibility have been implemented to ease future unit development . Main programmability/flexibility are listed in the following chapters.

7.1 Detector management

- Pixel period (from 100KSps to 3MSps) and associated high frequency master clock period
- Base time selection : Local Oscillator or external master clock selection (for several unit synchronization)
- CCD or CMOS sequencing selection
- Bias and clock levels digitally adjustable

7.2 Acquisition characteristics

- SpaceWire packet length is programmable from 200 to 4000 pixels
- Acquisition length : it is possible to program through SpaceWire the quantity of line that have to be acquired in operational mode before to return automatically in no video data mode
- SpaceWire speed : Fmax=100Mbps, Fmax/2, Fmax/4 and Fmin=10Mbps

7.3 Video Chain

- Input multiplexer control can be selected in VASP (controlled directly through SpaceWire) or externally (input multiplexer sequenced by HIVAC core sequencer)
- CDS and ADC sampling times are adjustable (step from pixel period/16 to pixel period/256)
- Pre-clamp clock is fully adjustable
- Black pixel envelop (for optical black regulation loop) is fully adjustable
- Multisampling per pixel can be selected for noise optimization
- Video chain gain is programmable through SpaceWire from 1 to 8 (3bits) . HIVAC core sequencer can also select video chain gain at line rate through VASP I^2C interface.

7.4 Optical black correction

- 3 modes are selectable for optical black correction : convergence mode to reach quickly the selected video offset (black level at ADC output), the regulating mode to maintain the video offset to the offset selected level and the constant mode freezing the applied correction value independently of the selected offset level.
- Two regulating loop are available in parallel inside VASP (one for each channel)
- Programmable parameter for the regulation loop are : Selected offset level, coarse offset corrections and integrator length of regulation algorithm
- VASP optical black correction can be managed externally through VASP I^2C interface

7.5 Specificity of HIVAC breadboard

Of course, HIVAC breadboard integrates specific programmability associated to the management of the selected detectors, in particular :

- § CCD55-20 readout mode : full frame or µband (with µband addresses and length programming)
- § ULIS µbolometer serial link programming

8 HIVAC BREADBOARD FEATURES

At this time, HIVAC breadboard place and route is on going. PCB area is estimated between 10000mm^2 and 13000mm^2. Fig. 5 gives an HIVAC breadboard illustration.

8.1 Connectors

Table 4 shows HIVAC breadboard connector list.

Table 4 : HIVAC breadboard connector list

Interface name	Connector Size
Power supply interface	MicroD 15pins
CCD interface	MicroD 25pins
µbolometer interface	MicroD 25pins
SpaceWire interface	MicroD 9pins
External clock interface	SMA
Test interface	MicroD 51pins

8.2 Power supplies

Table 5 shows HIVAC breadboard power supply list

Table 5 : HIVAC breadboard power supply list

Voltage	Load
33V	CCD bias
16.5V	CCD phase drivers
6V	CMOS bias
3.8V	CMOS bias and CCD phase drivers
1.5V	FPGA array
5V	DC correction, DAC and slow chains
-5V	DC correction and slow chain
3.3V	Digital
3.3V	VASP analog part

Future flight models based on HIVAC design and driving only one detector should need less than 7 secondary supplies.

8.3 Power consumption

Table 6 shows typical HIVAC breadboard Power budget.

Table 6 : HIVAC breadboard power budget

Blocks	Power consumption
HIVAC generic part	1200mW
CCD interface blocks	550mW
µbolometer interface blocks	130mW
Total (without focal plan)	1880mW

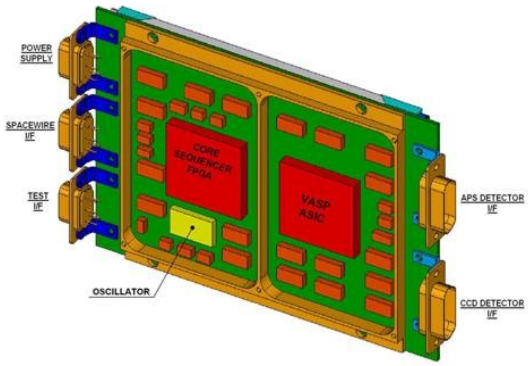

Fig. 5 : HIVAC breadboard illustration

8.4 HIVAC performances

Table 6 gives an extraction of main HIVAC performances with typical power supplies and a 3MSps conversion rate. Typical values are given at 25°C.

Table 6 : Main HIVAC electrical characteristics

PARAMETER & CONDITION	Min	Typ	Max	Unit
Temperature range				
Full perf. temperature range (Drift in temp. range of 30°C)	-30		80	°C
Video interface (At VASP level)				
Input Voltage range	0.2		3.1	V
Differential Video amplitude		4		V
Pseudo Diff. Video amplitude		2		V
Sample Rate	0.1		3	Msps
Gain accuracy		1		%
Gain drift (30°Cpp) after thermal adjustment		400		ppm

PARAMETER & CONDITION	Min	Typ	Max	Unit
Pseudo Diff. Interface for CCD (At preamplification level)				
Input Voltage range before clamping	0		30	V
Video amplitude		2		V
Reset Amplitude			0.7	V
Clamping Voltage range	0		4	V
Clamping capacitor		1		µF
Gain accuracy		1.5		%
Gain drift (30°Cpp) after thermal adjustment		450		ppm
Preamplifier gain (defined by resistors)		2	16	V/V
Preamplifier bandwidth			21	MHz
Pseudo Diff. Interface for µbolometer (At preamplification level)				
Input Voltage range	0		4.2	V
Video amplitude		2		V
DC correction range	0		4	V
Input impedance	200			kΩ
Input capacitance			15	pF
Gain accuracy		1.5		%
Gain drift (30°Cpp) after thermal adjustment		450		ppm
Preamplifier gain (defined by resistors)		2	16	V/V
Preamplifier bandwidth			21	MHz
Housekeeping (4 analog telemetries at VASP level)				
Input Voltage range	0		3	V
Input Voltage range	0.1		3	Msps
Gain stability			0.1	%
Accuracy / resolution		10		bits
VASP reference DACs (2 analog outputs)				
Number of bits		6		bits
DAC output range	0.2		3.1	V
DAC LSB		45		mV
PGA				
Number of bit		3		bits
Gain range	1		8	V/V
Radiometric performances with Pseudo diff connection to VASP (without pre-amplifier)				
Number of bits		16		bits
DNL	0.5		1	LSB
INL			1	LSB
Input referred Noise		2		LSB
Radiometric performances with Pseudo diff connection to pre-amplifier / DC correction stage				
Number of bits		16		bits
DNL	0.5		1	LSB
INL		1.5	3	LSB
Input referred Noise		2.25		LSB

PARAMETER & CONDITION	Min	Typ	Max	Unit
Optical Black correction				
Coarse correction range (of full scale)		10		%
Fine correction regulation range	-128		+128	LSB
Fine correction resolution			0.25	LSB
Offset Instruction programming range	0		1023	LSB
Offset loop integrator length programming range	1		255	LSB
SpaceWire Interface				
Data Rate User to VASP	2		100	Mbps
Data Rate VASP to User	2		100	Mbps

9 CONCLUSION

HIVAC and VASP architecture are issued from a detailed analysis performed in parallel on :

- § the state-of-the-art of monolithic CCD processor
- § The specifications of future observation missions
- § The characteristics of a wide range of detectors

The HIVAC project organization merging experience of MIPS/CHIPIDEA (analog and mixed IP provider) and THALES ALENIA SPACE (European leader on high resolution instruments for space) allowed to converge during phase 1 of the HIVAC project on an optimized definition and specification covering a wide range of applications in terms of functionalities and performances.

The actual detailed design of VASP and HIVAC is on going and critical design reviews are expected for both before the end of 2008. A full characterisation of VASP and HIVAC is foreseen over 2009.

The large programmability/flexibility of the HIVAC and the design of functional bricks constituting HIVAC breadboard will make easy the development of future flight units based on HIVAC/VASP design.

10 ACKNOWLEDGMENTS

THALES ALENIA SPACE Toulouse is in charge of the HIVAC project management and associated technical coordination. Nevertheless, HIVAC and VASP definition and feasibility study would not be successful without the contribution of MIPS/CHIPIDEA for their experience on complex mixed ASIC, THALES ALENIA SPACE Cannes for observation instrument expertise and THALES ALENIA SPACE Milan for HIVAC detailed design and development. Thanks to all teams which are still working on detailed design and development. Of course, we also acknowledge ESA for their confidence and support given in the frame of the HIVAC project.