PROCEEDINGS OF SPIE

Design for Manufacturability through Design-Process Integration VI

Mark E. Mason John L. Sturtevant Editors

15–16 February 2012 San Jose, California, United States

Sponsored and Published by SPIE

Volume 8327

Proceedings of SPIE, 0277-786X, v. 8327

SPIE is an international society advancing an interdisciplinary approach to the science and application of light.

Design for Manufacturability through Design-Process Integration VI, edited by Mark E. Mason, John L. Sturtevant, Proc. of SPIE Vol. 8327, 832701 · © 2012 SPIE · CCC code: 0277-786X/12/\$18 · doi: 10.1117/12.928432 The papers included in this volume were part of the technical conference cited on the cover and title page. Papers were selected and subject to review by the editors and conference program committee. Some conference presentations may not be available for publication. The papers published in these proceedings reflect the work and thoughts of the authors and are published herein as submitted. The publisher is not responsible for the validity of the information or for any outcomes resulting from reliance thereon.

Please use the following format to cite material from this book:

Author(s), "Title of Paper," in Design for Manufacturability through Design-Process Integration VI, edited by Mark E. Mason, John L. Sturtevant, Proceedings of SPIE Vol. 8327 (SPIE, Bellingham, WA, 2012) Article CID Number.

ISSN 0277-786X ISBN 9780819489838

Published by **SPIE** P.O. Box 10, Bellingham, Washington 98227-0010 USA Telephone +1 360 676 3290 (Pacific Time) · Fax +1 360 647 1445 SPIE.org

Copyright © 2012, Society of Photo-Optical Instrumentation Engineers

Copying of material in this book for internal or personal use, or for the internal or personal use of specific clients, beyond the fair use provisions granted by the U.S. Copyright Law is authorized by SPIE subject to payment of copying fees. The Transactional Reporting Service base fee for this volume is \$18.00 per article (or portion thereof), which should be paid directly to the Copyright Clearance Center (CCC), 222 Rosewood Drive, Danvers, MA 01923. Payment may also be made electronically through CCC Online at copyright.com. Other copying for republication, resale, advertising or promotion, or any form of systematic or multiple reproduction of any material in this book is prohibited except with permission in writing from the publisher. The CCC fee code is 0277-786X/12/\$18.00.

Printed in the United States of America.

Publication of record for individual papers is online in the SPIE Digital Library.



SPIEDigitalLibrary.org

Paper Numbering: Proceedings of SPIE follow an e-First publication model, with papers published first online and then in print and on CD-ROM. Papers are published as they are submitted and meet publication criteria. A unique, consistent, permanent citation identifier (CID) number is assigned to each article at the time of the first publication. Utilization of CIDs allows articles to be fully citable as soon as they are published online, and connects the same identifier to all online, print, and electronic versions of the publication. SPIE uses a six-digit CID article numbering system in which:

- The first four digits correspond to the SPIE volume number.
- The last two digits indicate publication order within the volume using a Base 36 numbering system employing both numerals and letters. These two-number sets start with 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B ... 0Z, followed by 10-1Z, 20-2Z, etc.

The CID number appears on each page of the manuscript. The complete citation is used on the first page, and an abbreviated version on subsequent pages. Numbers in the index correspond to the last two digits of the six-digit CID number.

Contents

- vii Conference Committee
- ix Introduction

KEYNOTE SESSION

- 8327 03 Implications of triple patterning for 14nm node design and patterning (Keynote Paper) [8327-02]
 K. Lucas, Synopsys, Inc. (United States); C. Cork, Synopsys, Inc. (France); B. Yu, Univ. of Texas (United States); G. Luk-Pat, B. Painter, Synopsys, Inc. (United States); D. Z. Pan, The Univ. of Texas at Austin (United States)
- 8327 04 Yield enhancement with DFM (Keynote Paper) [8327-03]
 S. W. Paek, J. H. Kang, N. Ha, B.-M. Kim, D. H. Jang, J. Jeon, D. Kim, K. Y. Chung, S. Yu, J. H. Park, S. Bae, D. Song, W. Noh, Y. Kim, H. Song, H. Choi, K. S. Kim, K.-M. Choi, W. Choi, J. Jeon, J. Lee, K.-S. Kim, S. Park, N.-Y. Chung, K. Lee, Y. Hong, B. Kim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

DFDP: DESIGN FOR DOUBLE PATTERNING

- 8327 05 Layout optimization through robust pattern learning and prediction in SADP gridded designs
 [8327-04]
 J.-Y. Wuu, Univ. of California, Santa Barbara (United States); M. Simmons, Mentor Graphics
 Corp. (United States); M. Marek-Sadowska, Univ. of California, Santa Barbara (United States)
- 8327 06 Self-aligned double patterning (SADP) compliant design flow [8327-05]
 Y. Ma, GLOBALFOUNDRIES Inc. (United States); J. Sweis, Cadence Design Systems, Inc. (United States); H. Yoshida, Y. Wang, J. Kye, H. J. Levinson, GLOBALFOUNDRIES Inc. (United States)
- 8327 07 **Design friendly double patterning** [8327-06] E. Yesilada, STMicroelectronics (France)
- 8327 08 Pattern matching for double patterning technology-compliant physical design flows
 [8327-07]
 L. T.-N. Wang, V. Dai, L. Capodieci, GLOBALFOUNDRIES Inc. (United States)

DESIGN RULES AND ROUTING

Basign-of-experiments based design rule optimization [8327-08]
 A. A. Kagalwalla, Univ. of California, Los Angeles (United States); S. Muddu, L. Capodieci, GLOBALFOUNDRIES Inc. (United States); C. Zelnik, Sagantec Inc. (United States); P. Gupta, Univ. of California, Los Angeles (United States)

- Fully integrated litho aware PnR design solution [8327-09]
 C. Beylier, STMicroelectronics (France); C. Moyroud, Mentor Graphics Corp. (France);
 F. Bernard Granger, F. Robert, E. Yesilada, Y. Trouiller, J.-C. Marin, STMicroelectronics (France)
- 8327 OB **Replacing design rules in the VLSI design cycle** [8327-10] P. Hurley, K. Kryszczuk, IBM Zürich Research Lab. (Switzerland)
- 8327 0C Smart double-cut via insertion flow with dynamic design-rules compliance for fast new technology adoption [8327-11]
 A. Abdulghany, R. Fathy, Mentor Graphics Corp. (United States); L. Capodieci, P. Pathak, S. Madhavan, S. Malik, GLOBALFOUNDRIES Inc. (United States)
- 8327 0D Local loops for robust inter-layer routing at sub-20 nm nodes [8327-12]
 W. Huang, D. Morris, Carnegie Mellon Univ. (United States); N. Lafferty, L. Liebmann, IBM Corp. (United States); K. Vaidyanathan, Carnegie Mellon Univ. (United States); K. Lai, IBM Corp. (United States); L. Pileggi, A. J. Strojwas, Carnegie Mellon Univ. (United States)

DESIGN IMPLEMENTATION AND VARIABILITY

- 8327 OE **A primer of physical design for lithographers (Invited Paper)** [8327-13] C.-M. Yuan, Freescale Semiconductor, Inc. (United States)
- 8327 OF Analysis, quantification, and mitigation of electrical variability due to layout dependent effects in SOC designs [8327-14]
 Y. Wang, M. Zwolinski, Univ. of Southampton (United Kingdom); A. Appleby, M. Scoones, S. Caldwell, T. Azam, Cambridge Silicon Radio Ltd. (United Kingdom); P. Hurat, Cadence Design Systems, Inc. (United States); C. Pitchford, Cadence Design Systems, Inc. (United Kingdom)
- 8327 0H **Design level variability analysis and parametric yield improvement methodology** [8327-16] R. März, M. Keck, Intel GmbH (Germany)
- 8327 01 Analysis of layout-dependent context effects on timing and leakage in 28nm [8327-17] P. McGuinness, Fastada (United States); P. Sharma, Freescale Semiconductor, Inc. (United States); P. Hurat, Cadence Design Systems, Inc. (United States)
- 8327 0J Variability aware compact model characterization for statistical circuit design optimization [8327-18]

Y. Qiao, K. Qian, C. J. Spanos, Univ. of California, Berkeley (United States)

JOINT SESSION WITH CONFERENCE 8326

Basign and manufacturability tradeoffs in unidirectional and bidirectional standard cell layouts in 14nm node [8327-19]
K. Vaidyanathan, S. H. Ng, D. Morris, Carnegie Mellon Univ. (United States); N. Lafferty, L. Liebmann, IBM Corp. (United States); M. Bender, W. Huang, Carnegie Mellon Univ. (United States); K. Lai, IBM Corp. (United States); L. Pileggi, A. Strojwas, Carnegie Mellon Univ. (United States)

- A novel methodology for triple/multiple-patterning layout decomposition [8327-21]
 R. S. Ghaida, Univ. of California, Los Angeles (United States); K. B. Agarwal, L. W. Liebmann,
 S. R. Nassif, IBM Corp. (United States); P. Gupta, Univ. of California, Los Angeles (United States)
- 8327 0N Overlay, decomposition and synthesis methodology for hybrid self-aligned triple and negative-tone double patterning [8327-22]
 W. Kang, Y. Chen, Peking Univ. (China)
- 8327 00 Computational lithography work flows and design rule exploration automation [8327-23]
 S. Sethi, W. Stanton, K. Lucas, J. Hiserote, Synopsys, Inc. (United States); D. Hur, R. Choi, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

SESSION 8 HOTSPOTS, CMP, AND FILL

- 8327 OP Thickness-aware LFD for the hotspot detection induced by topology [8327-24] J.-H. Kang, N. Ha, J.-H. Park, B.-M. Kim, S. W. Paek, H. Choi, K. S. Kim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); A. Mohy, S. Abdelwahed, M. Imam, Mentor Graphics Consulting Division (Egypt)
- 8327 0Q The complexity of fill at 28nm and beyond [8327-25]
 N. Rodriguez, J. Yang, Advanced Micro Devices, Inc. (United States); B. Graupp, J. Wilson, E. Anikin, Mentor Graphics Corp. (United States)
- 8327 0S In-design process hotspot repair using pattern matching [8327-27]
 D. Jang, N. Ha, J. Jeon, J.-H. Kang, S. W. Paek, H. Choi, K. S. Kim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Y.-C. Lai, P. Hurat, W. Luo, Cadence Design Systems, Inc. (United States)
- 8327 0T Clean pattern matching for full chip verification [8327-28]
 S. Nakamura, Toshiba Corp. (Japan); T. Matsunawa, Toshiba Corp. R&D Ctr. (Japan);
 C. Kodama, T. Urakami, N. Furuta, Toshiba Corp. (Japan); S. Kagaya, Toshiba
 Microelectronics Corp. (Japan); S. Nojima, Toshiba Corp. R&D Ctr. (Japan); S. Miyamoto,
 Toshiba Corp. (Japan)

POSTER SESSION

- 8327 0U Framework for identifying recommended rules and DFM scoring model to improve manufacturability of sub-20nm layout design [8327-29]
 P. Pathak, S. Madhavan, S. Malik, L. T.-N. Wang, L. Capodieci, GLOBALFOUNDRIES Inc. (United States)
- 8327 0V
 Self-aligned double and quadruple patterning layout principle [8327-30]
 K. Nakayama, C. Kodama, T. Kotani, Toshiba Corp. (Japan); S. Nojima, S. Mimotogi, Toshiba Corp. R&D Ctr. (Japan); S. Miyamoto, Toshiba Corp. (Japan)
- 8327 0W In-design hierarchical DFM closure for DFM-clean IP [8327-31]
 V. Tripathi, Freescale Semiconductor India (India); J. Subramanian, P. Sharma, Freescale Semiconductor, Inc. (United States); K.-H. Chen, B. Kasthuri, P. Hurat, L. Layton, Cadence Design Systems, Inc. (United States)

- Automated yield enhancements implementation on full 28nm chip: challenges and statistics [8327-32]
 S. Malik, S. Madhavan, P. Pathak, L. Capodieci, GLOBALFOUNDRIES Inc. (United States); R. Fathy, A. Abdulghany, Mentor Graphics Corp. (United States)
- A study of pattern variability for device performance [8327-33]
 T.-H. Kim, D.-H. Han, A.-R. Hong, Y.-H. Kim, J.-S. Lee, Y.-H. Chu, K.-J. Lee, Y.-J. Park, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)
- 8327 0Z Intra-cell process variability and compact modeling of LWR effects: from self-aligned multiple patterning to multiple-gate MOSFETs [8327-34]
 Y. Chen, W. Kang, Q. Cheng, Peking Univ. (China)
- 8327 10 Consideration of correlativity between litho and etching shape [8327-35]
 R. Matsuoka, H. Mito, Hitachi High-Technologies Corp. (Japan); S. Shinoda, Y. Toyoda, Hitachi Research Lab., Hitachi Ltd. (Japan)
- Advanced techniques for design assembly and characterization for the 14nm node with LFD using a black box API [8327-36]
 J. Opitz, A. Torres, Mentor Graphics Corp. (United States); I. Graur, IBM Corp. (United States); W. Manhawy, S. Kanodia, Mentor Graphics Corp. (United States); M. Shafee, S. Mohamed, A. Hassand, Mentor Graphics Corp. (Egypt); J. Bickford, IBM Corp. (United States)
- Fast optical proximity correction with timing optimization ready standard cells [8327-39]
 Y. Qu, C. H. Heng, A. Tay, T. H. Lee, National Univ. of Singapore (Singapore)
- 8327 15 Electrical design for manufacturability and lithography and stress variability hotspot detection flows at 28nmn [8327-40]
 P. Hurat, Cadence Design Systems, Inc. (United States); J. Zhu, E. Teoh, GLOBALFOUNDRIES Singapore (Singapore)
- 8327 16 Yield impacting systematic defects search and management [8327-41]
 J. Zhang, Q. Xu, X. Zhang, X. Zhao, J. Ning, Semiconductor Manufacturing International Corp. (China); G. Cheng, S. Chen, G. Zhang, Anchor Semiconductor, Inc. (China);
 A. Vikram, B. Su, Anchor Semiconductor, Inc. (United States)
- 8327 17 Model-based searching method to find the integrated critical failure on the wafer [8327-43]
 B.-S. Kang, N.-Y. Chung, H.-K. Park, S.-J. Lee, J.-H. Ku, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)
- A scoring methodology for quantitatively evaluating the quality of double patterning technology-compliant layouts [8327-44]
 L. T.-N. Wang, S. Madhavan, S. Malik, P. Pathak, L. Capodieci, GLOBALFOUNDRIES Inc. (United States)

Author Index

Conference Committee

Symposium Chairs

Donis G. Flagello, Nikon Research Corporation of America (United States)Harry J. Levinson, GLOBALFOUNDRIES Inc. (United States)

Conference Chair

Mark E. Mason, Texas Instruments Inc. (United States)

Conference Cochair

John L. Sturtevant, Mentor Graphics Corporation (United States)

Program Committee

Robert Aitken, ARM Inc. (United States) Jason P. Cain, Advanced Micro Devices, Inc. (United States) Luigi Capodieci, GLOBALFOUNDRIES Inc. (United States) Juan-Antonio Carballo, Netlogic Microsystems Inc. (United States) Fang-Cheng Chang, Cadence Design Systems, Inc. (United States) Lars W. Liebmann, IBM Corporation (United States) Andrew Neureuther, University of California Berkeley (United States) David Z. Pan, The University of Texas at Austin (United States) Chul-Hong Park, SAMSUNG Electronics Co., Ltd. (Korea, Republic of) Larry Pileggi, Carnegie Mellon University (United States) Michael L. Rieger, Synopsys, Inc. (United States) Vivek K. Singh, Intel Corporation (United States) Chi-Min Yuan, Freescale Semiconductor, Inc. (United States)

Session Chairs

- Keynote Session
 Mark E. Mason, Texas Instruments Inc. (United States)
 John L. Sturtevant, Mentor Graphics Corporation (United States)
- 2 DFDP: Design for Double Patterning
 Lars W. Liebmann, IBM Corporation (United States)
 Vivek K. Singh, Intel Corporation (United States)
- 3 Design Rules and Routing Andrew R. Neureuther, University of California, Berkeley (United States) Luigi Capodieci, GLOBALFOUNDRIES Inc. (United States)

- Design Implementation and Variability
 Rob Aitken, ARM Inc. (United States)
 Michael L. Rieger, Synopsys, Inc. (United States)
- 5 Optical/DFM: Joint Session with Conference 8326 Mark E. Mason, Texas Instruments Inc. (United States) Will Conley, Dynamic Intelligence (United States)
- Joint Session with Conference 8326
 John L. Sturtevant, Mentor Graphics Corporation (United States)
 Kafai Lai, IBM Corporation (United States)
- Hotspots, CMP, and Fill
 Chul-Hong Park, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)
 Jason P. Cain, Advanced Micro Devices, Inc. (United States)

Introduction

I am very excited to be writing this introduction to the Proceedings of the 2012 SPIE conference on Design for Manufacturability through Design-Process Integration (DfM-DPI).

This marks the sixth year of the DfM-DPI conference, and I could not be happier with the quality of work that was submitted for publication this year. Experts from around the world participated representing various segments of the Semiconductor industry and academia. Once again, we enjoyed strong representation from Europe, Asia, and America. We even saw an increase in participation (as measured by paper submissions) over last year, indicating that the industry remains heavily focused on Design for Manufacturability.

Our keynote speakers this year were simply outstanding. Well recognized as premier experts in their field, the presenters addressed critical manufacturability issues facing us during the coming transition to EUV, complications inherent in triple patterning; and successful approaches to using DfM as part of an overall yield enhancement strategy.

The depth of the technical sessions was also impressive, covering a wide range of topics. Emphasis on double patterning implications was apparent this year, as you might expect given current industry trends. An invited tutorial presentation describing the design flow (tailored to lithographers) was particularly well received. Other topics of note included design rule implications, place and route impact to DfM and variability.

One highlight of the event was the joint session with the Optical Lithography conference. Recognizing the powerful overlap between computational lithography topics like OPC and SMO, two joint sessions were presented featuring papers of mutual interest to both conferences. The standing-room-only crowd is clear evidence that this sort of inter-conference collaboration should continue in the future. Special thanks to the Optical guys for making this happen.

The bottom line is that the conference was very successful by any measure. As a personal note, I would like to thank the authors and conference attendees for their active participation: this conference if for you, and you make it happen.

Of course none of this would be possible without the generous support (and patience) of my co-chair (John Sturtevant of Mentor Graphics) and SPIE staff. Further, I deeply appreciate the efforts of the conference program committee for all their help in putting the program together and chairing sessions.

Together with these excellent people, I am already working hard to put together an even better program for 2013. I cannot wait to see you there.

Mark E. Mason John L. Sturtevant