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ROIC DEVELOPMENT AT CEA FOR SWIR DETECTORS: PIXEL CIRCUIT ARCHITECTURE AND TRADE-OFFS

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I. INTRODUCTION

Infrared detection is widely used in astrophysics and plays a key role in several space missions aiming for example at scanning the sky to discover new objects (coolest stars, dust-obscured galaxies, exo-planets …) or studying the evolution of the universe, where light is redshifted in the infrared range. In many cases the space telescope involves an HgCdTe infrared detector operating at low frame rate over long integration time. Due to the very low input signal, dark current and readout noise are essential figures that must be minimized to get the best detector sensitivity. This kind of application also requires very large focal plane array (FPA) often relying on a butting arrangement of large detectors [1]. The trend is to increase the single detector format from 1Kx1K to 2Kx2K and 4Kx4K. For very large formats, material quality and detector process may affect the production yield and the global infrared FPA cost. As a result the detector format could result from a trade-off taking into account producibility.

In the first part, we review three common pixel circuits and discuss their characteristics with respect to these application needs. In the second part we describe a ROIC based on SFD pixel that we have developed at CEA-LETI. Then we provide in the third part test results and electrical performances of the ROIC.

II. PIXEL CIRCUITS

Fig. 1 shows the schematics of Source-Follower per Detector (SFD), Direct Injection (DI) and Capacitive Trans-Impedance Amplifier (CTIA) pixel circuits. These are the more frequent input stages for hybrid detectors over the whole infrared spectrum. They all perform the same basic functions: photocurrent integration on a capacitive element and voltage readout through a switched source-follower buffer. Contrary to SFD, DI and CTIA also provide an – almost – constant photodiode bias voltage.
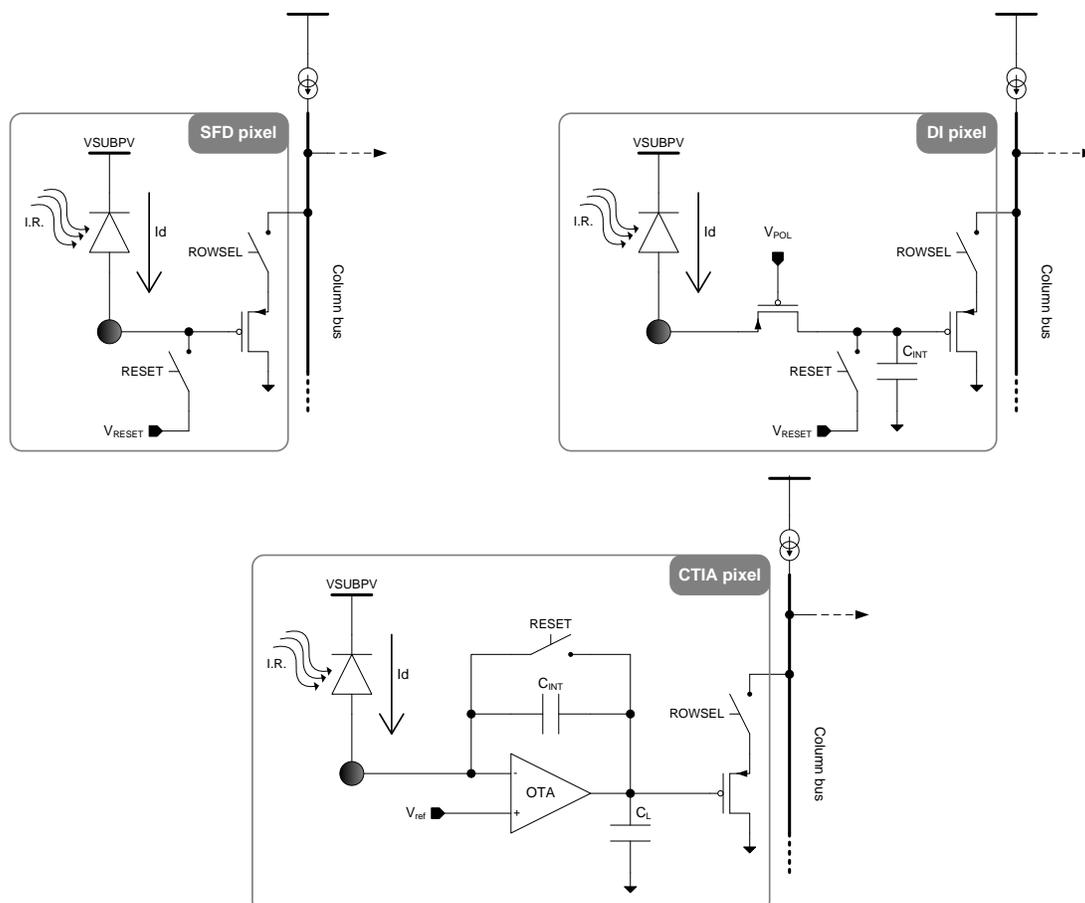

Fig. 1. Simplified diagrams of SFD, DI and CTIA pixel circuits.

A. Source-Follower Detector

In a SFD circuit the current is directly integrated on the input node capacitance after a reset (in a similar way to a 3T visible pixel). The integration node voltage is then read through a pixel switched source-follower that shares with other pixels a common current source. This output buffer stage drives the load capacitance which can be quite high in case of large array.

The integration capacitance is the sum of photodiode junction capacitance, MOS capacitance and metal interconnect capacitance. As the diode junction is generally the greater term, the nodal capacitance value varies with the voltage and leads to a non-linear characteristics which is one of the main drawbacks of SFD pixel. The non-constant photodiode biasing also raises several issues as Inter-Pixel Capacitance (IPC) effects [2]. The photodiode is not decoupled from the circuit and its bias voltage may be affected by electrical effects (coupling, charge injection) occurring on the high-impedance input node during readout.

Apart from reset noise which may be removed by Correlated Double Sampling (CDS) or other multiple sampling technics, the source-follower is the only noise contributor at pixel level. The total output noise related to the thermal noise can be easily derived from the small-signal model [3] and is given by (1) where γ is a constant related to device sizing and biasing. The readout noise can be quite low, especially on large arrays, thanks to a high load capacitance and in case of low readout speed, the bandwidth requirement can still be reached with limited power consumption.

$$\overline{V_{n,SF}^2} = \frac{\gamma kT}{C_L} \qquad (1)$$

Compared to other circuits, this pixel type will provide the lowest output noise voltage. This statement must be moderated by the fact that the charge-to-voltage conversion factor (CVF) would be lower. Indeed, the integration capacitance cannot be made as small as desired since it is dominated by the photodiode junction. So, when comparing the readout noise expressed in electrons, SFD may suffer from this lower conversion factor.

B. Direct Injection

In a direct injection circuit, we find the same output source-follower structure but the integration node is decoupled from the photodiode thanks to a common gate MOS stage. An integration capacitance is added in the pixel and its value can be adjusted independently for higher CVF. For the same readout chain noise, it will provide a better noise performance in electrons. The main drawback of this stage is that the current injection efficiency [4] depends on the photocurrent (I_d) via the MOS trans-conductance (g_m) as seen on (2). Since the MOS operates in weak inversion regime its trans-conductance is directly proportional to the current.

$$\eta_{inj} = \frac{I_{out}}{I_{in}} = A_{inj} \times \frac{1}{1+s\frac{R_d C_d}{1+g_m R_d}} \quad \text{with} \quad A_{inj} = \frac{g_m R_d}{1+g_m R_d} \quad \text{and} \quad g_m \approx \frac{I_d}{nkT/q} \qquad (2)$$

At low photocurrent, the MOS trans-conductance becomes very low independently of the transistor sizing. As a result, the gain term A_{inj} of the above equation drops. For a typical 15µm-pitch SWIR HgCdTe diode the dynamic resistance (R_d) ranges from 10^{12} to 10^{16} ohms for temperatures below 120K. Corresponding injection gain and cutoff frequency are plotted on fig. 2. It can be seen that a very high dynamic resistance is required to get a good injection gain at ultra-low input current but it leads at the same time to a low cutoff frequency setting a lower limit to the integration time. Finally, a minimum current of 1fA is needed to get a good gain with a dynamic resistance above 10^{14} ohms (which can be achieved in SWIR at 80K) at reasonable integration time with respect to application needs. This solution is not well suited for ultra-low flux astrophysics applications, which could involve only few electrons per second per pixel (i.e. less than 10^{-18} A).
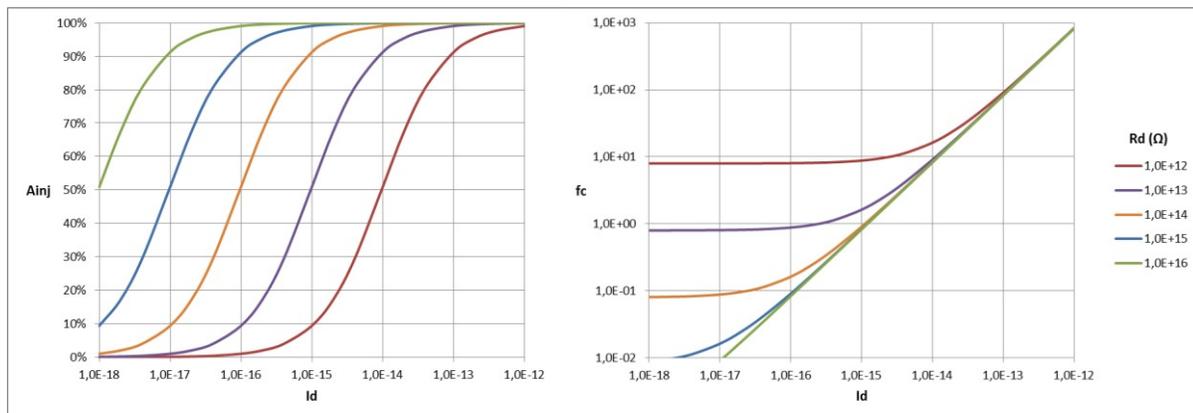

Fig. 2. DI injection gain and cutoff frequency in case of standard photodiode.

Nevertheless, Avalanche PhotoDiode (APD) technology may move this current boundary since avalanche gain (M) amplifies the photocurrent (I_{ph}) and offers a different dynamic resistance characteristic. In the avalanche regime (above a certain bias voltage, V_o) the gain has an exponential dependency with the bias voltage (3). It can be derived (4) that the $g_m.R_d$ product will approximately be independent of the photocurrent and bias voltage thus giving a constant injection gain.

$$I_d(V) = M(V) \cdot I_{ph} \quad \text{with} \quad M(V) \approx e^{a(V-V_o)} \quad \text{where } a \text{ and } V_o \text{ are two constants.} \tag{3}$$

$$g_m \cdot R_d = \frac{g_m}{\frac{\partial I_d(V)}{\partial V}} \approx \frac{M(V) \cdot I_{ph}}{\frac{\partial M(V)}{\partial V} I_{ph} \cdot nkT/q} \approx \frac{q}{ankT} \tag{4}$$

Using a more precise electrical model for the APD diode [5] we also performed circuit simulations that confirm the previous analysis. Coupling an APD with a direct injection pixel gives injection gain above 99% even at low current (10^{-18} A) and low gain. Compared to standard photodiode, the cutoff frequency when no gain is applied is similar to what we obtained with very high dynamic resistance values (we don't have the floor frequency behavior that occurred for lower R_d). As the APD gain has a direct effect on the current flowing through the MOS it helps improving its trans-conductance and at the end the cutoff frequency.
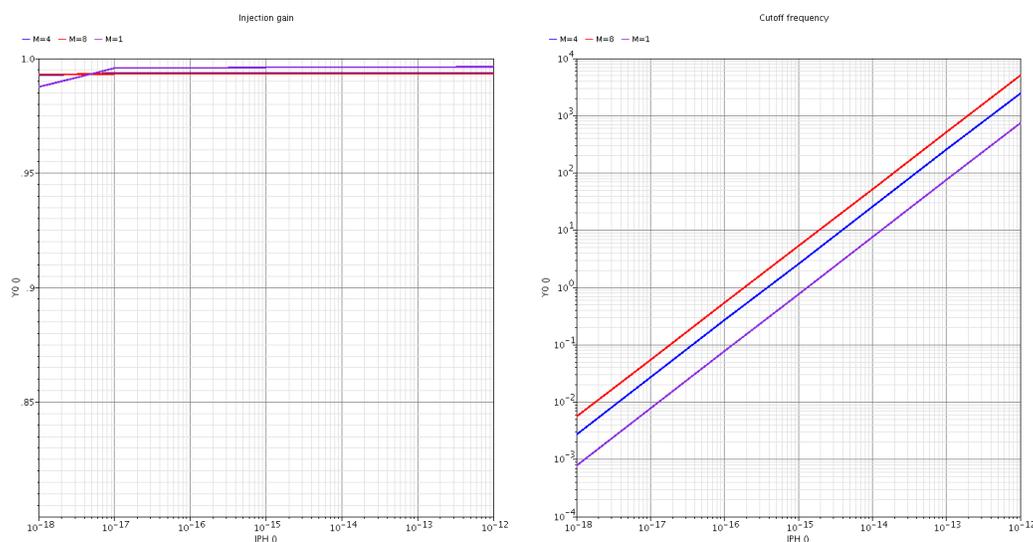

Fig. 3. DI injection gain and cutoff frequency in case of avalanche photodiode.

Concerning the noise, APD will slightly degrade the BLIP SNR due to its excess noise factor (about 1.2) but it will reduce the readout noise contribution in electrons thanks to a higher CVF than a SFD pixel (due to smaller integration capacitance and/or APD gain).

To summarize, while DI is not well suited for very-low flux SWIR applications with a standard photodiode, the use of an avalanche photodiode gives a high and constant injection gain, greater than 99%. Thus, it could be an interesting alternative with good noise performance, especially for large arrays with small pixels (10μm and below) to avoid IPC and other coupling effects. Considering a moderate gain for the SWIR APD (M<10), the cutoff frequency remains low and would limit its use to some applications with very long integration time or higher current. Also, further work is needed to reach dark current and space reliability requirements with this emerging technology.

C. Capacitive Trans-Impedance Amplifier
This circuit allows adjusting the CVF in the same way, offers a precise low-impedance photodiode bias but without the injection efficiency issue of DI pixel. We performed a noise analysis to evaluate the interest of a CTIA input stage. The amplifier noise contribution can be added as a voltage source at the input. The noise transfer function (5) can be calculated from the small signal circuit [3].

$$NTF(s) = \frac{V_{n,out}}{V_{n,in}} = \left(1 + \frac{Cin}{Cint}\right) \times \frac{1}{1+s.g_m/C_{eq}} \quad \text{with} \quad C_{eq} = \frac{C_{in}C_{int}+C_{in}C_l+C_{int}C_l}{C_l} \tag{5}$$

For this analysis, we extracted simulation data (trans-conductance, input thermal and flicker noise) from a real CTIA circuit. The output noise was then calculated for a variable feedback capacitor by applying the noise transfer function. CDS is necessary for low noise performance as it removes the large reset noise. In a pixel with strong area constraints, the amplifier flicker noise is the dominant noise contributor and integration time will determine the final noise value as it modifies the spectral response of CDS filtering.

The readout chain after the integration node (pixel source follower, output buffer) will add a constant voltage noise (B). Its value will mainly depend on the chain bandwidth and power consumption limitations. We can consider that a CTIA pixel becomes beneficial compared to SFD when the feedback capacitance is small enough so that the reduction of the readout chain noise due to higher conversion gain compensates the extra pixel noise due to the amplifier. We plotted on fig. 4 the CDS read noise evolution with the CTIA feedback capacitance for three different readout chain noise values and for three different integration times. We also plotted the results without considering the flicker noise. In order to enable a comparison with SFD we added data points showing the noise of the readout chain converted to electrons considering a 30fF nodal capacitance.
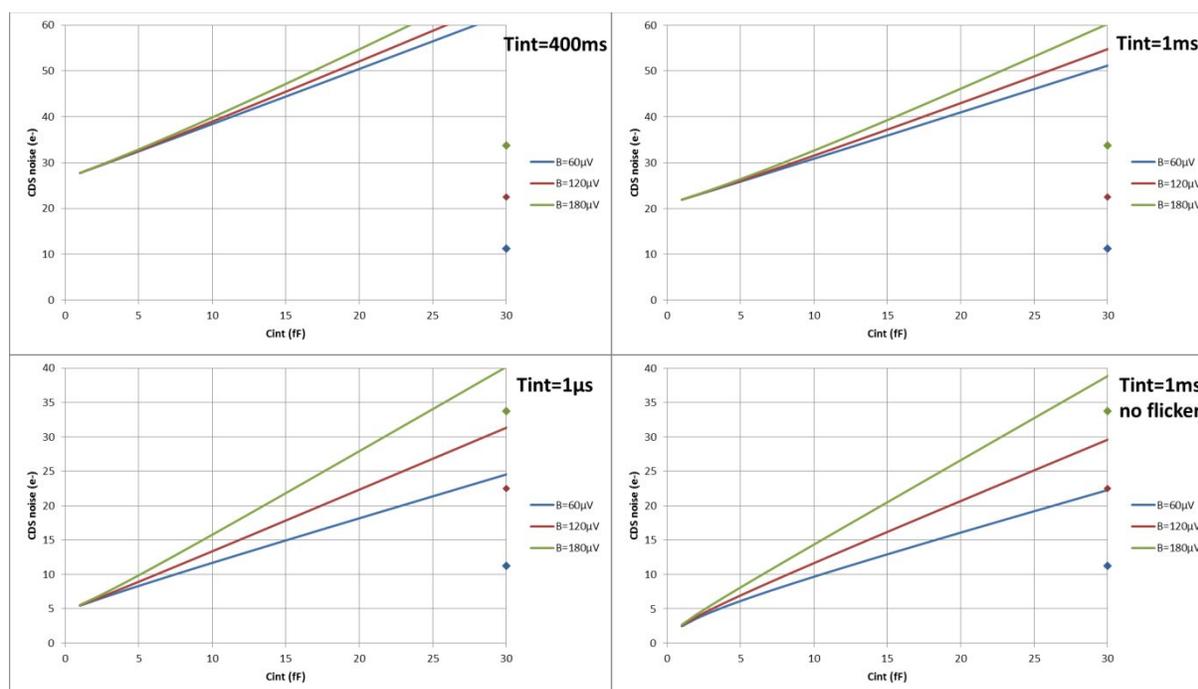

Fig. 4. Noise analysis results of a CTIA pixel.

In the targeted applications, the readout speed is very low. As a result, the readout chain bandwidth can be small leading to low noise values (typically below 100μV). In these conditions, a CTIA will give higher noise especially because with long integration time the flicker noise of the amplifier will remain significant after CDS. Low-frequency noise on the reference voltage (in case of differential structure) or power supply (in case of single-ended structure) could further increase the noise of the CTIA.

Beside noise, the amplifier power consumption is also a key issue as it can reach 50mW to 150mW for large format arrays (eg. 1Kx1K to 2Kx2K). Careful power supply routing over the array is required and special design technics can be used to minimize or compensate gradients due to I-R drop. In addition, the pixel-level amplifier can cause hot carrier injection (HCI) or thermal emission which is critical for glow-sensitive, low-flux applications.

From this analysis, it can be derived that CTIA is not well suited when targeting very low noise performance at slow readout speed. At video speed (50fps and above), it becomes an alternative solution since the higher conversion gain will decrease the effect of the higher readout chain noise while the CDS will be more effective at filtering the amplifier flicker noise and low frequency reference voltage noise. In this case low noise performance (<15e-) can be reached with high gain CTIA. It will typically be used in medium array size (up to 1Kx1K) where its power consumption remains acceptable.

III. SFD ROIC DEVELOPMENT

Following a previous development [6] from our partner, Sofradir, we designed a 640x512 ROIC with 15µm pixel-pitch in a standard 0.18µm CMOS process. It has been hybridized with a SWIR HgCdTe photodiode array in the perspective of astrophysics applications. Such ultra-low flux applications require low noise multiple readouts at a low rate (2.5fps) over very long integration time (several minutes). As discussed in the previous part, a SFD pixel is the good candidate and special care was taken during design to minimize the ROIC input capacitance, reduce the readout noise and limit the glow.

The circuit architecture is presented on fig. 5. The active pixel array is surrounded by a ring of four reference pixels which are not connected to a photodiode but to an equivalent capacitance on the ROIC. Several rows of test pixels have also been added for the purpose of electrical characterization. The array is divided into height strips that are read in parallel. Each strip is connected to an analog output buffer working at 110kHz. In SFD pixel, the photodiode voltage is not kept constant and inter-pixel capacitance could cause crosstalk between pixels. To enable the evaluation of IPC we included a test mode that keeps some hardwired pixels spread over the array under reset (red dots on the figure).
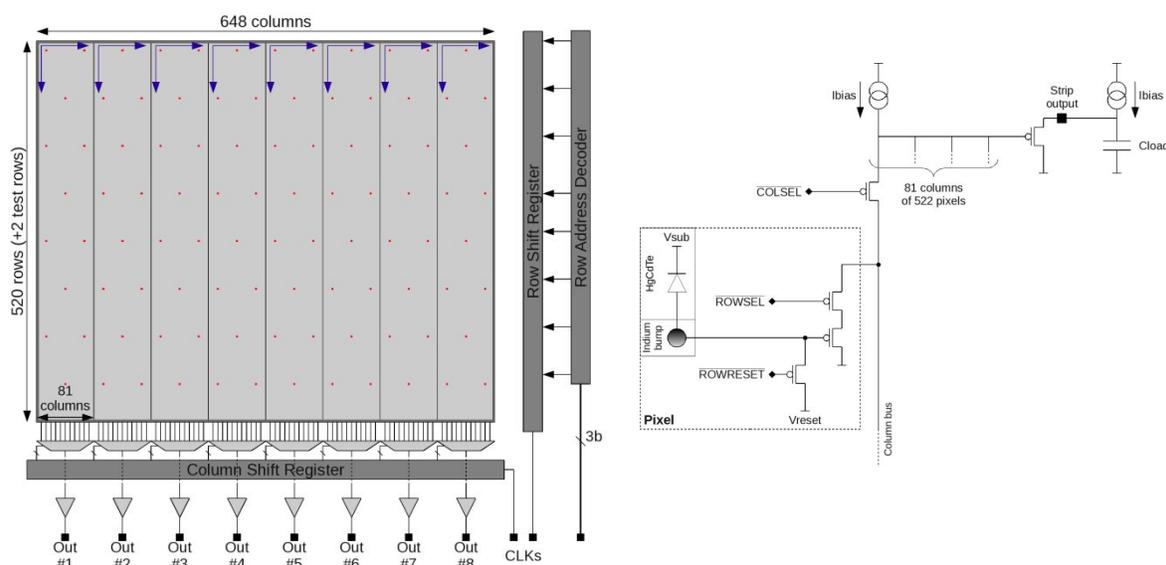

Fig. 5. ROIC architecture and simplified schematic.

As speed is not a concern here, standard cells based on minimum channel length MOS are not necessary. In order to minimize the HCI we designed custom gates with a sizing that reduces the electrical field across the transistor channel [7]. The register architecture based on half frequency clock also lowers the switching activity and digital power consumption. Shielding and guard rings have also been used to limit the glow.

The circuit includes a 3 bits row address decoder for basic windowing purpose. It allows much faster readout compared to the 400ms full frame readout time by choosing the starting row (window position) while the number of rows and columns to be read is adjustable (window size) with the control signals. In this mode the strips are still operated in parallel. The windowing mode is useful when the input current becomes high (above 10 fA), for example in case of photodiode characterization at high temperature.

IV. TEST RESULTS

One of the key parameter of the detector is the pixel nodal capacitance. It is interesting to evaluate the ROIC input capacitance (C_p) independently of the photodiode junction capacitance. The average input capacitance of the ROIC has been evaluated with three families of test pixels having fixed capacitances of 10, 15 and 20fF connected between the integration node and a reference voltage. One can measure the pixel capacitance by changing the reference voltage in the middle of an acquisition. The pixel capacitance is then given by:

$$\Delta V_{out} = \Delta V_{in} \times \frac{c_f}{c_f + c_p} \tag{6}$$

where C_f is the fixed capacitance of the test pixel, ΔVin is the voltage difference applied on the reference voltage and $\Delta Vout$ is the difference between the two measured signals. With this test method we obtained a 5.6fF ROIC capacitance which is noticeably small and fairly close to the expected design value.

We used a test pixel not connected to a photodiode but embedding an equivalent capacitance to measure the leakage current. Although there is a small uncertainty related to the measurement, we can see on fig. 6 that the leakage is about 0.04e-/s at 80K and quite steady up to 200K. This value meets the requirement but an improvement would be an objective for future developments in order to get some margin compared to SWIR photodiode dark current at low temperature.
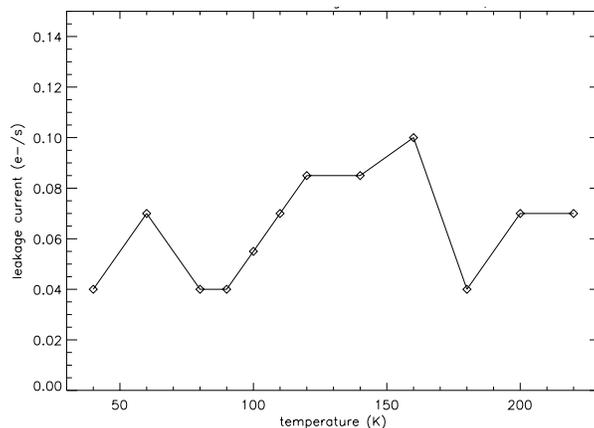

Fig. 6. ROIC leakage measurements.

A rms read noise of 50µV has been measured – including the acquisition electronics contribution – at 80K under continuous reset. In our test bench, the acquisition is based on 16 bits ADCs having an input referred rms noise of 35µV. We can thus infer a ROIC contribution of 36µV i.e. almost the same magnitude. The CDS noise was also measured on reference pixels based on two successive readouts (spaced in time by 0.4s). Fig. 7 shows that the CDS process is effective at removing the large reset noise (kT/C) while it increases the noise to 72µV – almost in the expected √2 ratio – compared to the previous continuous reset value. If we remove the acquisition electronics noise it leads to 52µV for the ROIC itself. Based on the 20.6fF nodal capacitance of test pixels it corresponds to a CDS noise of 9.3e- and 6.7e- respectively for an expected linear well around 60ke- when hybridized to a photodiode.
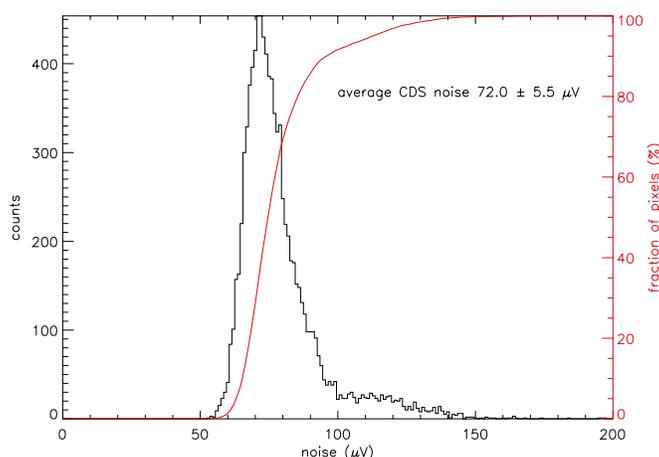

Fig. 7. CDS noise measurement at 80K for Tint=0.4s.

The noise was also evaluated with different multiple readout schemes representative of possible operating conditions: CDS with Tint=60s, FUR-150 with Tint=60s and Fowler-32 with Tint=600s. These measurements have been performed at 100K using test pixels with 20.6fF nodal capacitance. Fig. 8 illustrates the results and shows that a noise below 4e- (including acquisition electronics) can be obtained with FUR-150.
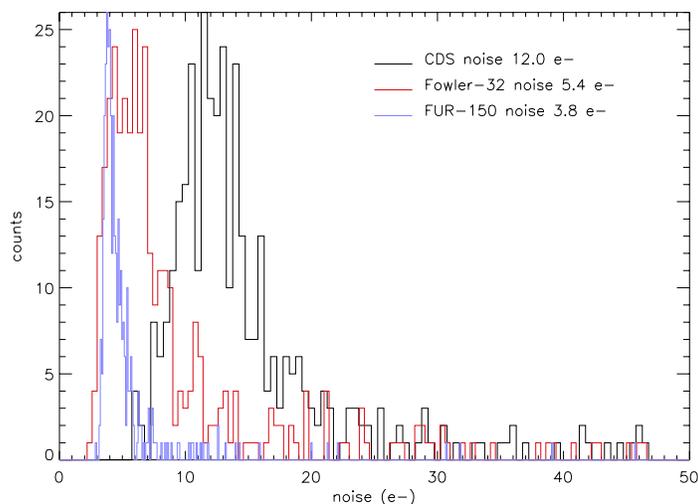
Fig. 8. Multiple sampling noise measurements at 100K.

The on-chip power consumption measured in typical operating conditions is detailed in table 1. The main consumption comes from the eight analog output buffers driving the large external load at 110kHz. It can be highlighted that the digital power consumption is extremely low (0.8μW). No glow effect has been observed on hybridized detectors.

Table 1. ROIC power consumption.

	Average current (μA)	Typical voltage (V)	Power consumption (μW)
Digital	0,5	1,8	0,8
Analog & line drivers	85,0	3,3	280,5
Output buffer	259,0	1	259,0
TOTAL	**344,5**		**540,3**

V. CONCLUSION

Our analysis confirmed that SFD is the good choice for ultra-low flux, glow-sensitive applications working at low frame rate. It is well suited for large arrays. While direct injection is useful to decouple the diode from the integration node and to allow pixel conversion factor adjustment independently of the diode junction capacitance it is not appropriate at very-low flux due to poor injection efficiency. But we showed that coupling this input stage to an avalanche photodiode constitutes a novel and interesting alternative, in particular for small pixels. It offers a very good current injection above 99% even with low APD gain and low current. The avalanche gain could help reducing the noise of the readout chain while increasing the input stage cutoff frequency. Anyway, in case of very-low flux this frequency remains low and limits this solution to applications with very long integration time. CTIA pixel will not have these limitations and is therefore a good solution for high frame rate applications. Compared to SFD, higher pixel conversion gain will mitigate the input-referred readout chain noise, for a global benefit when this noise reduction compensates the extra pixel's amplifier noise. A benefit will effectively be obtained with a small feedback capacitance (<10fF) in case and short integration time (<1ms) for proper flicker noise filtering through CDS. Power consumption would be an issue for very large arrays (above 1Kx1K) and a concern for glow.

As we targeted ultra-low flux applications, we developed a 15μm-pich 640x512 ROIC based on an SFD pixel. It was designed in the goal to minimize the ROIC input capacitance and glow effects. The CDS noise of the ROIC has been measured and is about 52μV at 80K. It corresponds to 6.7e- with a nodal capacitance value of 20.6fF on which the ROIC only contributes for 5.6fF. The pixel leakage current is about 0.04e-/s and no glow effect has been observed. The custom digital circuit's power consumption is very low (0.8μW) for a total of 540μW for the whole chip in normal operating conditions (full-frame readout at 2.5fps). These ROIC electrical results meet the high performance level required for SWIR infrared astrophysics applications while the circuit architecture is scalable for larger arrays.

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