# Micro/Nanolithography, MEMS, and MOEMS 

# Contact hole shrink process using graphoepitaxial directed self-assembly lithography 

Yuriko Seino<br>Hiroki Yonemitsu<br>Hironobu Sato<br>Masahiro Kanno<br>Hirokazu Kato<br>Katsutoshi Kobayashi<br>Ayako Kawanishi<br>Tsukasa Azuma<br>Makoto Muramatsu<br>Seiji Nagahara<br>Takahiro Kitano<br>Takayuki Toshima

# Contact hole shrink process using graphoepitaxial directed self-assembly lithography 

Yuriko Seino<br>Hiroki Yonemitsu<br>Hironobu Sato<br>Masahiro Kanno<br>Hirokazu Kato<br>Katsutoshi Kobayashi<br>Ayako Kawanishi<br>Tsukasa Azuma<br>Toshiba Corporation<br>Center for Semiconductor Research \& Development<br>1, Komukai Toshiba-cho, Saiwai-ku<br>Kawasaki 212-8583, Japan<br>E-mail: yuriko.seino@toshiba.co.jp

## Makoto Muramatsu

Tokyo Electron Kyushu Ltd.
1-1 Fukuhara, Koshi-City
Kumamoto 861-1116, Japan

## Seiji Nagahara

Tokyo Electron Ltd.
3-1 Akasaka 5-chome, Minato-ku
Tokyo 107-6325, Japan

## Takahiro Kitano

Takayuki Toshima
Tokyo Electron Kyushu Ltd.
1-1 Fukuhara, Koshi-City
Kumamoto 861-1116, Japan


#### Abstract

A contact hole shrink process using directed self-assembly lithography (DSAL) for sub-30 nm contact hole patterning is reported on. DSAL using graphoepitaxy and poly (styrene-block-methyl methacrylate) (PS-b-PMMA) a block copolymer (BCP) was demonstrated and characteristics of our process are spin-on-carbon prepattern and wet development. Feasibility of DSAL for semiconductor device manufacturing was investigated in terms of DSAL process window. Wet development process was optimized first; then critical dimension (CD) tolerance of prepattern was evaluated from three different aspects, which are DSA hole CD, contact edge roughness (CER), and hole open yield. Within $70+/-$ 5 nm hole prepattern CD, $99.3 \%$ hole open yield was obtained and CD tolerance was 10 nm . Matching between polymer size and prepattern size is critical, because thick PS residual layer appears at the hole bottom when the prepattern holes are too small or too large and results in missing holes after pattern transfer. We verified the DSAL process on a $300-\mathrm{mm}$ wafer at target prepattern CD and succeeded in patterning sub-30 nm holes on center, middle, and edge of wafer. Average prepattern CD of 72 nm could be shrunk uniformly to DSA hole pattern of 28.5 nm . By the DSAL process, CD uniformity was greatly improved from 7.6 to 1.4 nm , and CER was also improved from 3.9 to 0.73 nm . Those values represent typical DSAL rectification characteristics and are significant for semiconductor manufacturing. It is clearly demonstrated that the contact hole shrink using DSAL is a promising patterning method for next-generation lithography. © The Authors. Published by SPIE under a Creative Commons Attribution 3.0 Unported License. Distribution or reproduction of this work in whole or in part requires full attribution of the original publication, including its DOI. [DOI: 10.1117/1.JMM. 12 .3.033011]

Subject terms: directed self-assembly; graphoepitaxy; block copolymer; poly (styrene-block-methyl methacrylate); contact hole shrink; wet development.


Paper 13048P received Apr. 16, 2013; revised manuscript received Jun. 19, 2013; accepted for publication Jul. 10, 2013; published online Aug. 12, 2013.

## 1 Introduction

A new patterning technique capable of generating fine patterns is strongly anticipated for advanced semiconductor device manufacturing. ArF immersion single-patterning processes have already reached their resolution limit, and some semiconductor device manufacturers have already introduced the ArF immersion double-patterning processes. However, they require very complex process and the cost is surging. Although extreme ultraviolet lithography and nanoimprint lithography have better resolution than ArF immersion lithography, they are still facing many challenges with performance, throughput, and cost. Recently, directed selfassembly lithography (DSAL) is attracting attention as a low-cost and fine patterning method. DSAL has several technical and economic advantages over other technologies. It enables nanofabrication of line-and-space features below $20-\mathrm{nm}$ half-pitch using conventional lithography tools with lower cost of ownership.

We have already demonstrated the wet development process using poly (styrene-block-methyl methacrylate) (PS-$b$-PMMA) in combination with deep ultraviolet (DUV) exposure, which induces chain scission in the PMMA block to promote dissolution in developer solvent. ${ }^{1,2}$ The wet development process provides selective removal of PMMA block. It also provides more remaining of PS film, which
works as a mask on pattern transfer by reactive ion etching (RIE).

Contact hole shrink process using DSA is one of the most promising applications for semiconductor device manufacturing. It is expected to provide superior critical dimension uniformity (CDU) for contact holes $<30 \mathrm{~nm}$ in diameter. In this work, we investigate the feasibility of DSAL for semiconductor manufacturing in terms of DSAL process window. Through the correlation between hole prepattern CD and DSA hole pattern CD, the target prepattern CD was determined based on contact edge roughness (CER) and hole open yield. Some hole patterning processes have been proposed by DSAL such as chemoepitaxy using PMMA cylinders, ${ }^{3}$ pillars and spheres, ${ }^{4,5}$ template using PMMA cylinders, ${ }^{6,7,8}$ trench using PMMA cylinders, ${ }^{9}$ and resist prepattern using organic and Si blend polymer. ${ }^{10}$ In this paper, we demonstrated simple graphoepitaxy using hole-type prepatterns and cylinder-forming PS-b-PMMA block copolymer (BCP). The key points of our process are spin-oncarbon (SOC) prepattern and wet development. Prepattern material is required to have some special properties such as surface free energy control, solvent resistance to the solvent of BCP solution, thermal resistance on BCP anneal, etching resistance on pattern transfer, and so on. In previous works, guiding pattern materials such as silicon oxide ${ }^{8}$ and
negative tone development resist ${ }^{11}$ have been reported. We selected SOC as a guiding material from a cost and etching resistance point of view. Inorganic materials need more pattern transfer processes than SOC to form guide patterns. SOC has etching resistance on pattern transfer compared to resist. With respect to wet development, chain scission of PMMA is induced by DUV irradiation and the PMMA domain becomes selectively soluble to organic solvent. Wet development provides greater etching margin compared to dry development, which utilizes the difference of RIE rate between PS and PMMA. This is the reason we selected SOC prepattern and wet development.

## 2 Experimental

### 2.1 Materials

PS- $b$-PMMA diblock copolymer was supplied from Tokyo Ohka Kogyo Co., Ltd., Kawasaki, Japan. Commercially available ArF photoresist, spin-on-glass (SOG), and SOC were used.

### 2.2 Equipment

A CLEAN TRACK ${ }^{\text {TM }}$ ACT12 ${ }^{\text {TM }}$ (Tokyo Electron Ltd., Tokyo, Japan) was used for the SOC coating. A CLEAN TRACK ${ }^{\text {TM }}$ LITHIUS ${ }^{\text {TM }}$ (Tokyo Electron Ltd.) was used for the SOG and photoresist coating, baking, and development. An NSR-S308F (Nikon Corp., 0.92 NA, Saitama, Japan) ArF excimer laser scanner was used for exposures. BCP was coated and baked using a CLEAN TRACK ACT12 ${ }^{\text {TM }}$. DUV irradiation to the BCP films was performed by DUV ( $\lambda<200 \mathrm{~nm}$ ) exposure unit.

### 2.3 Metrology

SOC prepattern CD and DSA hole pattern CD were measured by CD-SEM (Hitachi CG4000). Cross-sectional images were taken by SEM (Hitachi S-5500).

### 2.4 Lithography Process

Graphoepitaxial DSAL process flow using SOC prepatterns and wet development is illustrated in Fig. 1. Stacked mask process (S-MAP), which utilizes a trilayer resist process consisting of resist, SOG, and SOC, was employed to obtain hole-type prepatterns in SOC layer. First, a silicon oxide film was deposited on a $300-\mathrm{mm} \mathrm{Si}$ wafer and SOC was spin-coated on the substrate to form an underlayer with a thickness of 100 nm . The SOG film was coated over the SOC layer with a thickness of 45 nm . A 120 -nm-thick layer of ArF photoresist was spin-coated on the SOG and baked. The resist hole patterns were formed by conventional

193 nm dry lithography [Fig. 1(a)]. The resist hole pattern
CD was 90 nm in diameter and the pattern pitch was 280 nm . Then, the resist hole patterns were transferred to SOC layer by using RIE to form hole-type prepatterns in SOC layer [Fig. 1(b)]. In this process step, the hole-type prepattern CD was reduced to 70 nm in diameter. A $1.5 \mathrm{wt} \%$ solution of PS-b-PMMA diblock copolymer (80.5 to $34.5 \mathrm{~kg} / \mathrm{mol}$ for PS and PMMA blocks, cylinder period $L_{0}=53.9 \mathrm{~nm}$, polydispersity index $=1.07$ ) dissolved in propylene glycol monomethyl ether acetate was spin-coated on the hole-type prepatterns and baked at $110^{\circ} \mathrm{C}$ for 60 s with a thickness of 100 nm . To induce microphase separation, thermal annealing was performed under the condition of $240^{\circ} \mathrm{C}$ for 60 s in $\mathrm{N}_{2}$ atmosphere [Fig. 1(c)]. Finally, PMMA cylindrical domain at the center of the hole-type prepatterns was selectively removed by the wet development process [Fig. 1(d)]. DUV ( $\lambda<200 \mathrm{~nm}$ ) was irradiated in $\mathrm{N}_{2}$ atmosphere to degrade the PMMA polymer chain, and then development was performed by immersing in organic solvent for 30 s .

## 3 Results and Discussion

### 3.1 Process Window of DSAL

As described above, the wet development consists of two process steps: DUV irradiation and organic solvent treatment. DUV irradiation condition was optimized. DUV ( $\lambda<200 \mathrm{~nm}$ ) was irradiated in $\mathrm{N}_{2}$ atmosphere to prevent attenuation, and the PMMA polymer chain scission was achieved effectively. The effect of DUV exposure dose on PMMA cylindrical domain removal was evaluated. The exposure dose was changed from 180 to $1800 \mathrm{~mJ} / \mathrm{cm}^{2}$. Then the wafer was developed by organic solvent for 30 s. Figure 2 shows top-down and cross-sectional SEM images after wet development. The dose condition in this study was chosen as $1800 \mathrm{~mJ} / \mathrm{cm}^{2}$.

In our DSAL process, the sidewall of the hole-type prepatterns was made of SOC and the bottom floor of the prepattern was made of silicon oxide. After resist patterns were transferred to S-MAP by RIE, the contact angles of the SOC sidewall and silicon oxide bottom are measured to be 49.0 and 38.0 deg , respectively. Since the contact angle of PMMA is 73 deg and that of PS is 93 deg , it is supposed that the sidewall and bottom floor of the prepatterns have an affinity for PMMA. So after microphase separation, thin film of PMMA layer would be formed along the prepattern surface as well as the cylindrical PMMA domain at the center of the prepatterns surrounded by PS domain. In the wet development, the cylindrical domains of PMMA were removed; however, the thin film of PMMA layer was not dissolved. We consider the thin PMMA layer to be too thin to be


Fig. 1 Contact hole shrink process using graphoepitaxial DSAL (a) ArF lithography. (b) Stacked mask process RIE. (c) BCP coating and microphase separation. (d) Wet development.


Fig. 2 Effect of DUV exposure dose on the PMMA cylindrical domain removal. Top-down and cross-sectional SEM images. Exposure doses are (a) $180 \mathrm{~mJ} / \mathrm{cm}^{2}$, (b) $360 \mathrm{~mJ} / \mathrm{cm}^{2}$, (c) $720 \mathrm{~mJ} / \mathrm{cm}^{2}$, (d) $1080 \mathrm{~mJ} / \mathrm{cm}^{2}$, and (e) $1800 \mathrm{~mJ} / \mathrm{cm}^{2}$, respectively.
removed because of the existence of an interfacial region between PS and PMMA domains.

In order to measure the process window of DSAL, the hole-type prepattern with different CDs in diameter ranging from 40 to 100 nm with $3-\mathrm{nm}$ steps were prepared by changing exposure dose of 193 nm ArF dry lithography in a 300mm wafer. The hole-type prepattern CD and DSA hole CD were measured over 15 holes/chip and compared. Figure 3 shows SEM photomicrographs of the hole-type prepatterns [Fig. 3(a)] and DSA holes [Fig. 3(b)]. The DSA hole shape was changed in accordance with the hole-type prepattern CD. When the hole-type prepattern CD was too small, BCPs was overflowed out of the hole type prepatterns [Fig. 3(b) to 3(i)]. At the optimum prepattern CD, shapes of DSA holes are circular [Fig. 3(b)(ii)]. But at the large prepattern CD, DSA holes shape became elliptical [Fig. 3(b)(iii)]. When the prepattern CD is much larger, doughnut-shaped
(lateral cylinder) were observed [Fig. 3(b)(iv)]. Correlation between the hole-type prepattern CD and the DSA hole CD is plotted in Fig. 4. When the hole-type prepattern CD is between 45 and 75 nm , DSA hole shape is circular (approximately the ratio of major/minor axis is 1.0 to 1.3 ) and DSA hole CD is slightly increasing but almost constant around 25 nm in diameter. On the other hand, when the prepattern hole CD is over 75 nm , the DSA hole shape is elliptical (approximately the ratio of major/minor axis is 1.5 to 1.8 ) and the DSA hole CD increases along with increment of the hole-type prepattern CD. CD tolerance of the hole-type prepattern in terms of DSA hole shape is $\sim 30 \mathrm{~nm}$.

CER of the hole-type prepattern and the DSA holes are shown in Fig. 5. CER was calculated by determining the center of the target hole pattern followed by calculating 3 sigma over 16 radii measured at different angles. Because the hole-type prepatterns were patterned by 193 nm ArF


Fig. 3 SEM photomicrographs of the hole-type prepatterns and DSA holes (a) hole-type prepattern and (b) DSA holes.


Fig. 4 Correlation between the hole-type prepattern critical dimension (CD) and the DSA hole CD.


Fig. 5 Contact edge roughness of the hole-type prepattern and the DSA holes.
dry lithography, CER of the hole-type prepatterns were very large and measured to be 3.5 nm . However, CER of the DSA holes was greatly improved to 0.6 nm . The CER improvement is a typical advantage of DSAL, since the roughness is often a critical issue in semiconductor device manufacturing. CD tolerance of the hole-type prepattern in terms of CER is $\sim 30 \mathrm{~nm}$.

Figure 6 shows hole open yield of the DSA holes. The hole-type prepattern with different CDs in diameter ranging from 40 to 100 nm with $3-\mathrm{nm}$ steps were also prepared in a $300-\mathrm{mm}$ wafer. The hole open yield of the DSA holes were investigated by using top-down SEM images over 15 holes/ chip and 3 chips/dose. Only circular holes were classified as "open" holes, whereas elliptical and overflowing holes were judged to be "missing" holes. The ratio of open holes to total ( $=$ open holes + missing holes) holes was defined as the hole open yield. In the region of the hole-type prepattern CD between 65 and $75 \mathrm{~nm}, 100 \%$ hole open yield was achieved. In the region of the hole-type prepattern CD under 65 nm , overflowing holes were observed. On the other hand, in the region of the hole-type prepattern CD over 75 nm , elliptical holes appeared, resulting in lower hole open yield. CD tolerance of the hole-type prepattern


Fig. 6 Hole open yield dependence on hole prepattern CD.
in terms of the hole open yield is $\sim 10 \mathrm{~nm}$ and the center of the hole-type prepattern CD is 70 nm . Hole open yield was also evaluated after pattern transfer to the silicon oxide film underneath. CD tolerance and center of the hole-type prepattern CD were consistent with those of the DSA holes.

CD tolerance of the hole-type prepattern for the hole open yield is narrower than that for the DSA hole CD (Fig. 4) and for the DSA hole CER (Fig. 5). The narrowness of the CD tolerance can be explained by the cross-sectional SEM images shown in Fig. 6. In the case of the overflowing and elliptical holes, a thick PS residual layer is formed on the bottom floor of the hole-type prepattern. The thick PS residual layer impedes pattern transfer using RIE and, as a result, holes are not formed in the silicon oxide film successfully. Therefore, considering CD tolerances described above, actual process window for device manufacturing is determined to be 10 nm . This process window is enough for semiconductor manufacturing.

### 3.2 Process Verification on 300 mm Wafer

Target CD of the hole-type prepatterns formed in SOC was determined to be 70 nm from the above-mentioned results. The DSAL process was verified on $300-\mathrm{mm}$ wafer. CDs were measured in 82 shots on 300 mm wafer. Top-down SEM images of hole-type prepatterns and DSA hole patterns on a $300-\mathrm{mm}$ wafer are shown in Fig. 7. Sub- 30 nm contact hole patterns were successfully fabricated across the $300-\mathrm{mm}$ wafer.

Comparison of CDUs between the hole-type prepatterns and the DSA hole patterns are shown in Fig. 8. Because of insufficient optimization of RIE conditions, intrawafer uniformity of the hole-type prepatterns formed in SOC was poor and their CDs at wafer edge region were larger than target CD [Fig. 8(a)]. Average CD of the hole-type prepatterns and that of the DSA hole patterns were measured to be 72.1 and 28.5 nm , respectively. By the DSAL process, CDU was greatly improved, from 7.6 to 1.4 nm . This represents a typical DSA rectification characteristic. Since CDU is important for semiconductor manufacturing, this is a major merit of DSAL.

Comparison of CER between the hole-type prepatterns and DSA hole patterns are shown in Fig. 9. Due to the insufficient optimization of the RIE, the prepatterns CER at wafer edge region were larger than the center region. CER was also improved from 3.9 to 0.73 nm . This result also represents the rectification capability of DSAL.


Fig. 7 Top-down SEM images of (a) prepattern and (b) DSA hole patterns on 300 mm wafer.


Fig. 8 CD uniformity of (a) prepattern and (b) DSA hole patterns on 300 mm wafer.


Fig. 9 Contact edge roughness of (a) prepattern and (b) DSA hole patterns on 300 mm wafer.


Fig. 10 Hole open yield on 300 mm wafers.

Finally, dispersion of the hole open yield on a $300-\mathrm{mm}$ wafer is evaluated. Two wafers were processed successively using the same condition and hole open yield was evaluated across the whole $300-\mathrm{mm}$ wafer in Fig. 10. Low yield at wafer edge region is due to large CD of the hole-type prepattern. This means that the DSAL is not responsible for the degradation of the hole open yield at the wafer edge region. Yields of $99.3 \%$ (average of two wafers and except the wafer edge region in which the hole-type prepattern CD is over 75 nm ) were successfully obtained.

## 4 Conclusion

Feasibility of DSAL for semiconductor device manufacturing was investigated in terms of DSAL process window. Wet development process was optimized and, by correlation between hole prepatterns and DSA hole patterns, the target CD was evaluated in terms of CD, CER, and hole open yield. Hole open yield of $99.3 \%$ was obtained at $70+/-5 \mathrm{~nm}$ hole prepattern CD. CD tolerance is 10 nm , sufficient for process window in semiconductor manufacturing. Matching between polymer size and prepattern size is critical, because PS residual layer of hole bottom in small or large hole prepattern is thicker than that in optimal hole prepattern, inducing the missing of holes.

We verified the DSAL process on a $300-\mathrm{mm}$ wafer at target prepattern CD and succeeded in patterning sub-30 nm holes on center, middle, and edge of wafer. Average CD of hole prepatterns of 72 nm could be shrunk uniformly to DSA hole patterns of 28.5 nm . By the DSAL process, CDU was greatly improved, from 7.6 to 1.4 nm , and CER was improved from 3.9 to 0.73 nm . Those values represent typical DSA rectification characteristics and are
significant for semiconductor device manufacturing. We are confident that DSAL is a promising patterning for next-generation lithography.

## References

1. M. Muramatsu et al., "Nanopatterning of diblock copolymer directed self-assembly lithography with wet development," J. Micro. Nanolithogr. MEMS MOEMS. 11(3), 031305 (2012).
2. Y. Seino et al., "Contact hole shrink process using directed selfassembly," Proc. SPIE 8323, 83230Y (2012).
3. R. Ruiz et al., "Density multiplication and improved lithography by directed block copolymer assembly," Science 321(5891), 936-939 (2008).
4. I. Bita et al., "Graphoepitaxy of self-assembled block copolymers on two-dimensional periodic patterned templates," Science 321(5891), 939-943 (2008).
5. C. A. Ross et al., "Templated self-assembly of Si-containing block copolymers for nanoscale device fabrication," Proc. SPIE 7637, 76370 H (2010).
6. L. Chang et al., "Experimental demonstration of aperiodic patterns of directed self-assembly by block copolymer lithography for random logic circuit layout," in Electron Devices Meeting (IEDM), 2010 IEEE International, 33.2.1-33.2.4 (2010).
7. H. Yi et al., "Flexible control of block copolymer directed self-assembly using small, topographical templates: potential lithography solution for integrated circuit contact hole patterning," Adv. Mater. 24(23), 3107-3114 (2012).
8. C. Bencher et al., "Directed self-assembly defectivity assessment," Proc. SPIE 8323, 832301N (2012).
9. S. Xiao et al., "Graphoepitaxy of cylinder-forming block copolymers for use as templates to pattern magnetic metal dot arrays," Science 16(7), 936-939 (2005).
10. Y. Hishiro et al., "Applications of DSA for lithography," in The SOKUDO Lithography Breakfast Forum (2012).
11. B. Rathsack et al., "Pattern scaling with directed self assembly through lithography and etch process integration," Proc. SPIE 8323, 83230B (2012).

Biographies and photographs of the authors are not available.

